An Introduction to Digital Signal Processing

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The Learning Curve

- Learning DSP can be a daunting experience
- Urgent need for a ‘Crystal Set’ approach to learning
- “Learn by doing” – DSP Lab

DSP Lab

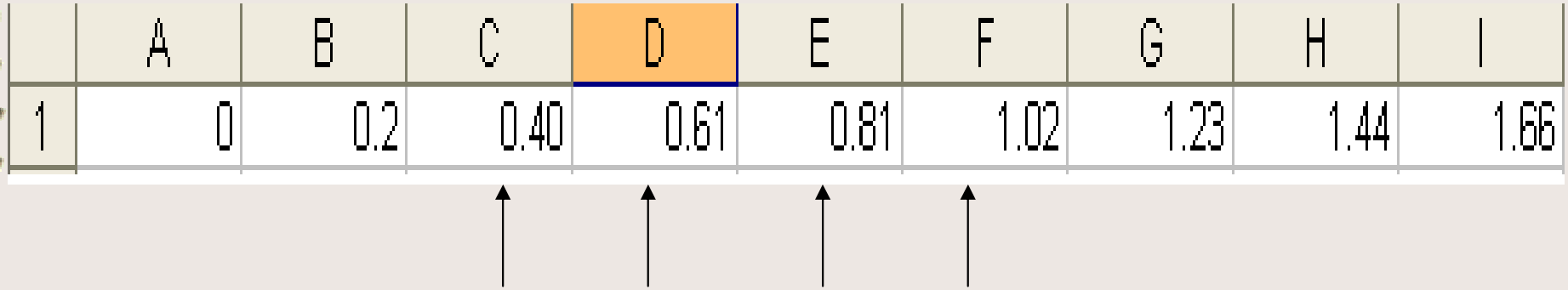
- Test Equipment
  - Analog to Digital Converter (ADC)
  - Digital to Analog Converter (DAC)
  - Oscilloscope
  - Signal Generator
    - CW, AM, FM, PSK31 etc
    - Sweep
    - I & Q outputs
  - Filters, highpass, lowpass and bandpass
  - Spectrum Analyzer

DSP Lab

- Assumptions:
  - You have a PC
  - We don't require 'real-time' results
- We can build all this test equipment using common software i.e.

DSP Lab

- Analog to Digital Converter



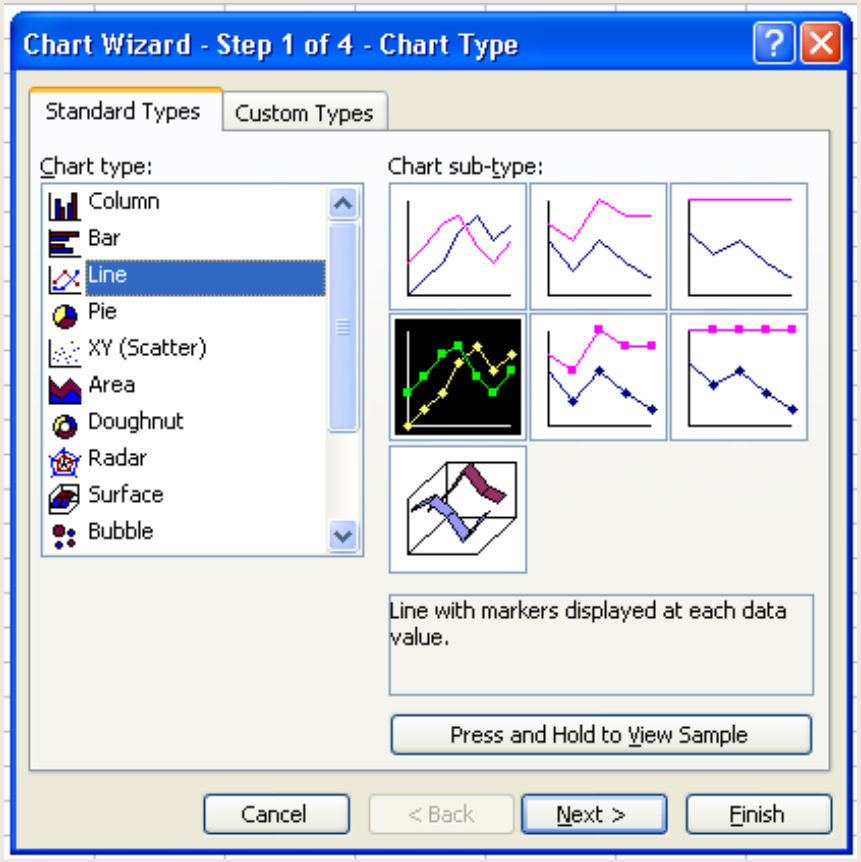
	A	B	C	D	E	F	G	H	I
1	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44	1.66

Each cell represents a sample

DSP Lab

- Digital to Analog Converter

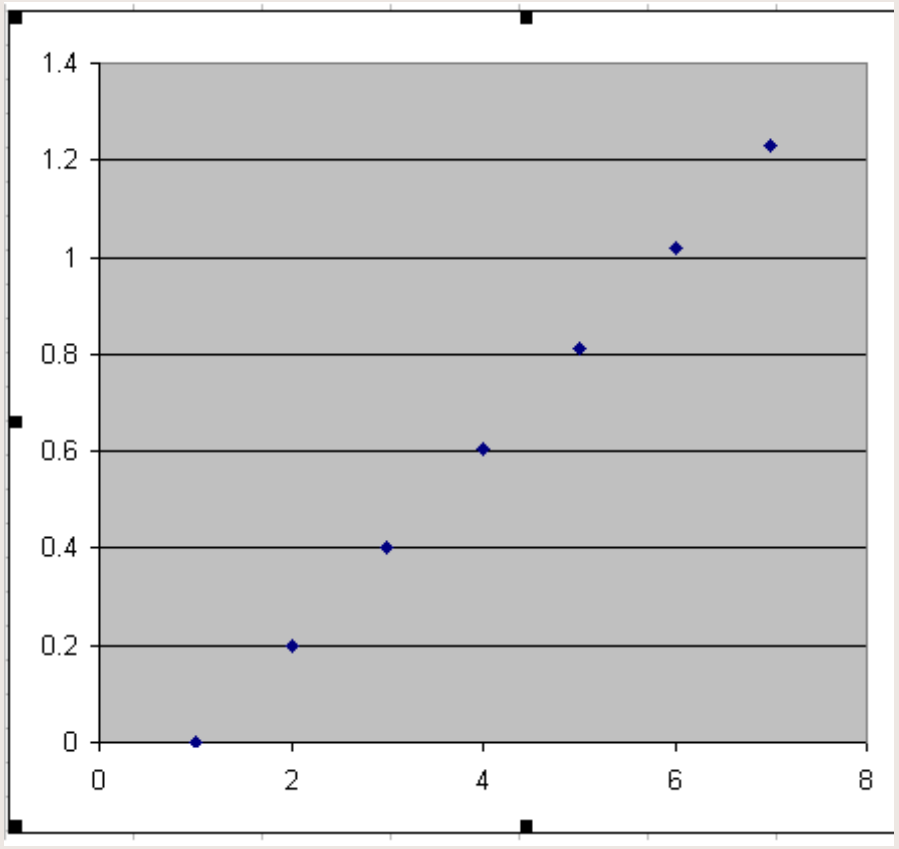
	A	B	C	D	E	F	G	H
1	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44



DSP Lab

- Digital to Analog Converter

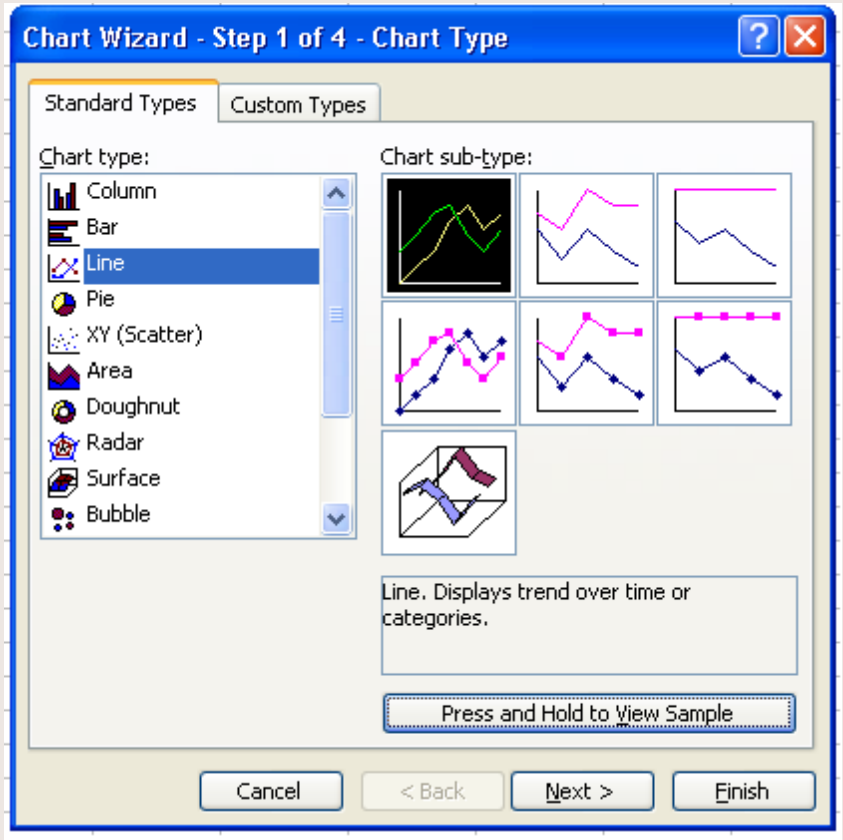
	A	B	C	D	E	F	G	H
1	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44



DSP Lab

- Digital to Analog Converter

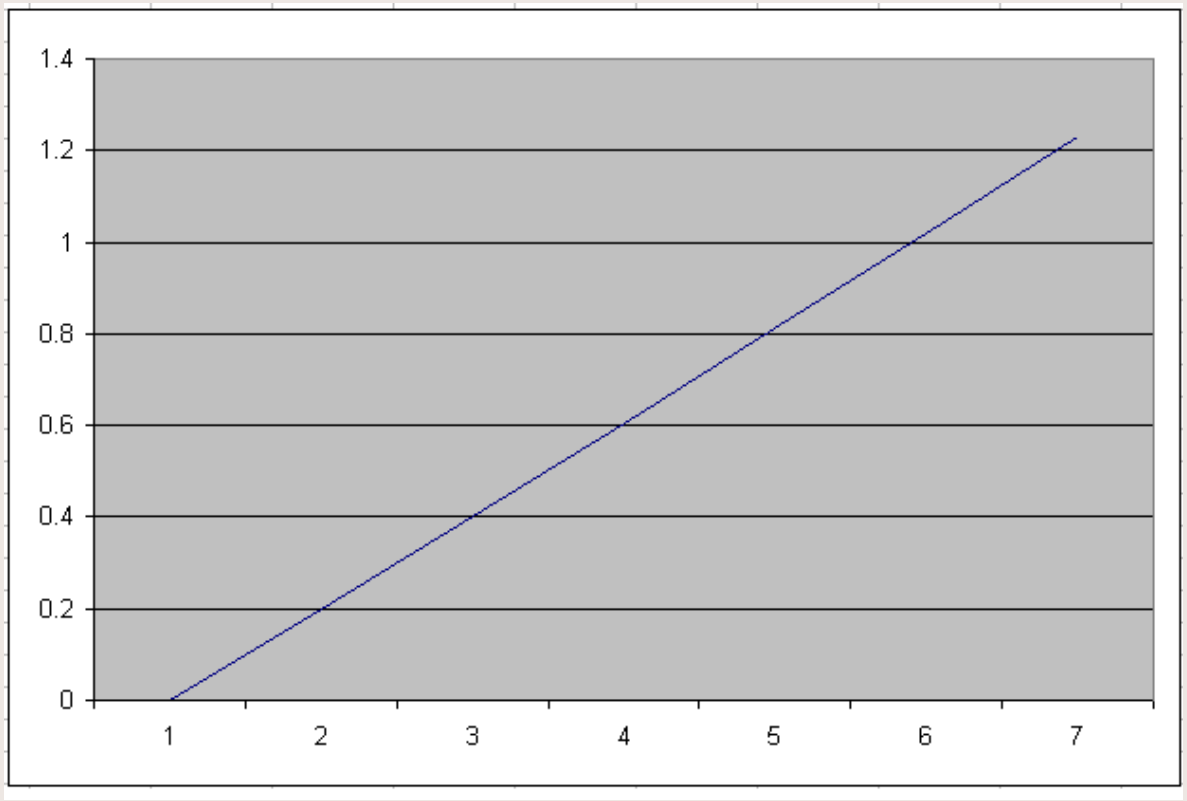
	A	B	C	D	E	F	G	H
1	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44



DSP Lab

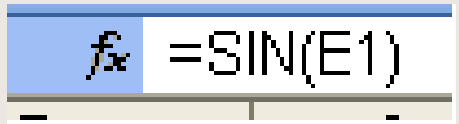
- Digital to Analog Converter (‘scope)

	A	B	C	D	E	F	G	H
1	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44

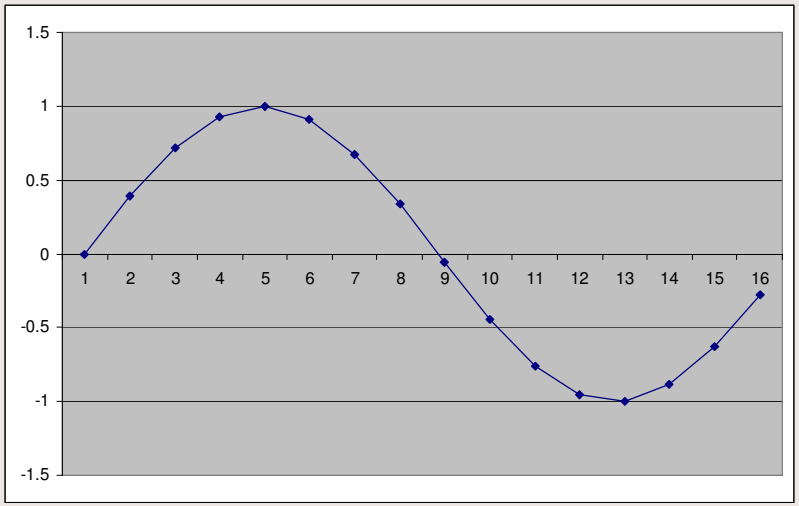


DSP Lab

- Signal Generator
  - Generate a sine wave - sin(angle)
  - in Excel



	A	B	C	D	E	F	G	H	I
1	angle	0	0.4	0.8	1.2	1.6	2	2.4	2.8
2	sine(angle)	0	0.389418	0.717356	0.932039	0.999574	0.909297	0.675463	0.334988



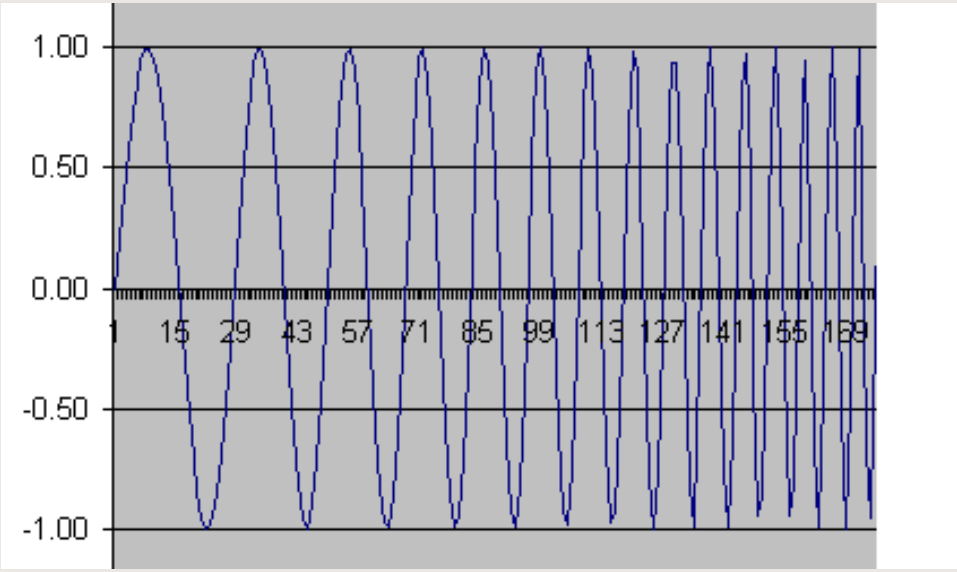
  - smaller increment = lower frequency

DSP Lab

- Sweep Generator
  - Add an increment to each angle

=0.2+ (B1*1.01)

	A	B	C	D	E	F	G	H	I	J	K
1	phase	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44	1.66	1.87
2	sin	0.00	0.20	0.39	0.57	0.73	0.85	0.94	0.99	1.00	0.95

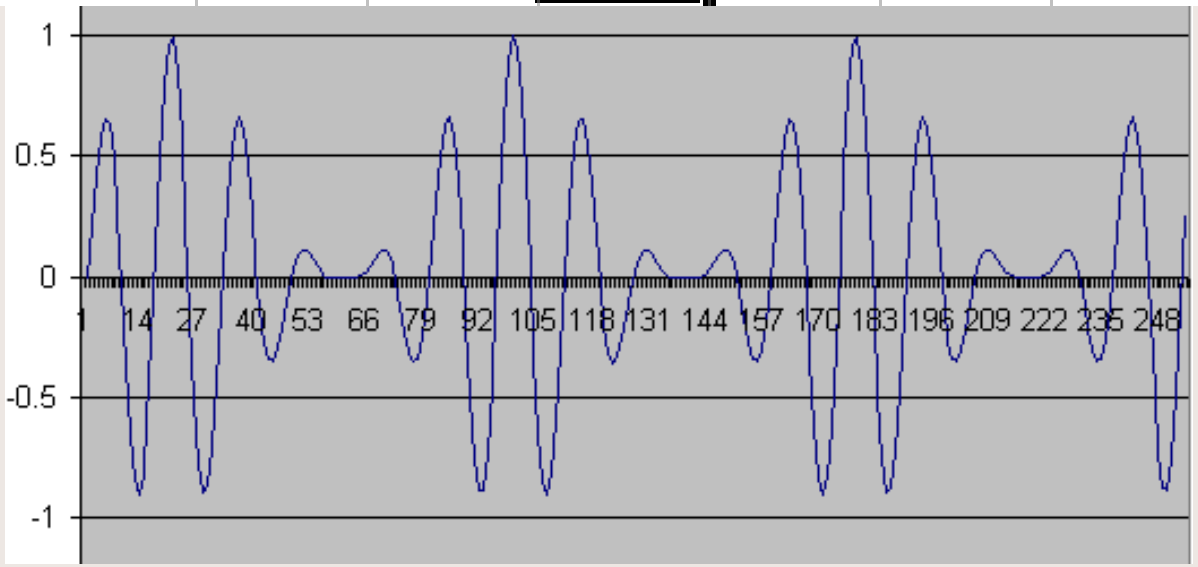


DSP Lab

- Signal Generator – AM
  - AM = 0.5(1 + m.Modulation)Carrier

D4 | f_x =0.5*((1 + D3)*D2)

	A	B	C	D	E	F	G
1		phase	0	0.4	0.8	1.2	1.6
2	10Khz carrier	sin	0	0.389418	0.717356	0.932039	0.999574
3	2kHz modulation	sin	0	0.079915	0.159318	0.237703	0.314567
4	AM		0	0.210269	0.415822	0.576794	0.657003

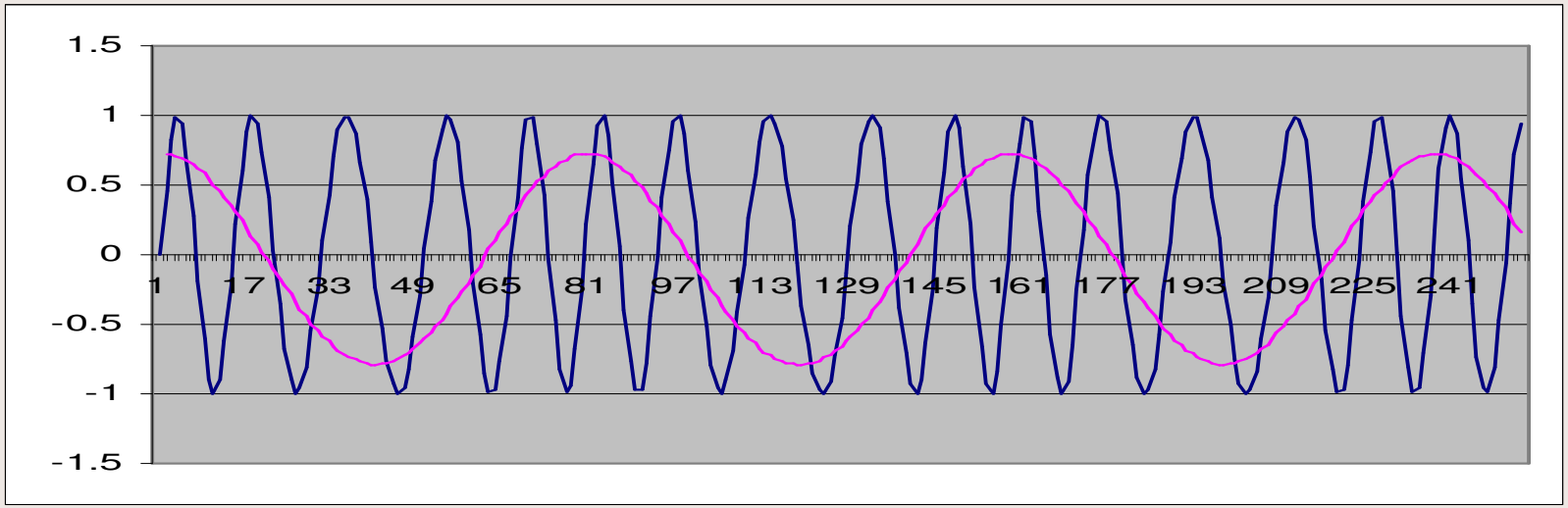


DSP Lab

- Signal Generator – FM
  - FM = sin(angle + β.Modulation)

D3 =SIN(D1+D2)

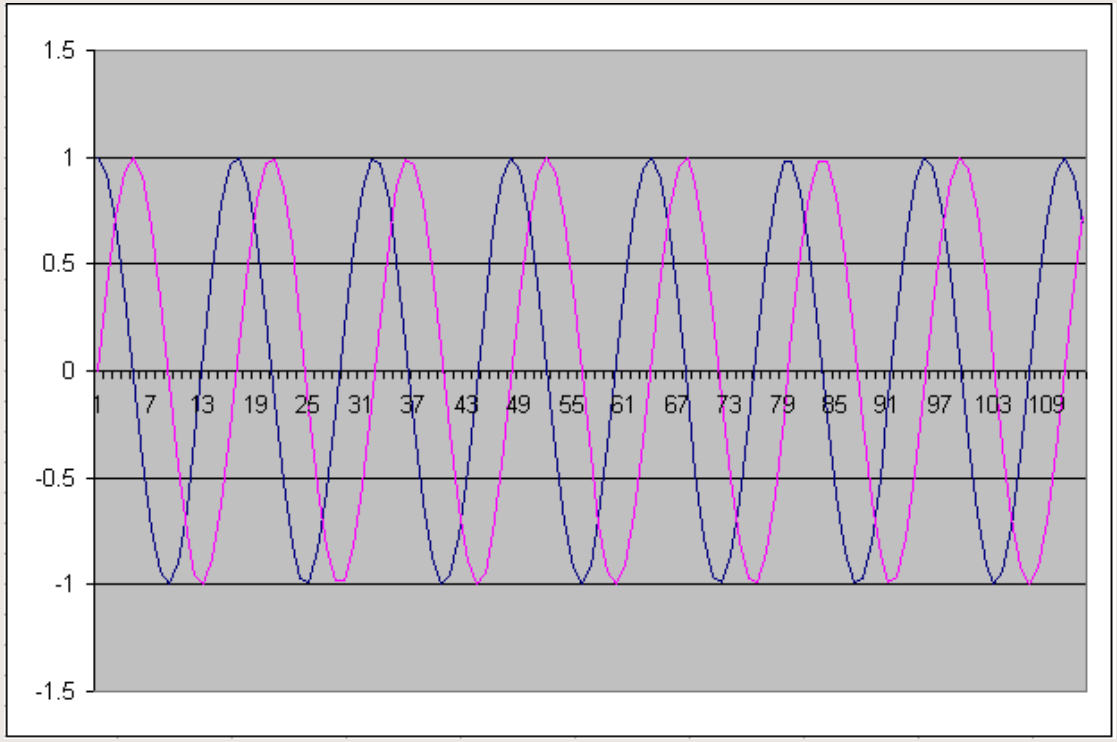
	A	B	C	D	E	F
1		phase	0	0.4	0.8	1.2
2	2kHz modulation	sin	0	0.079915	0.159318	0.237703
3	FM		0	0.461704	0.8188	0.991156



DSP Lab

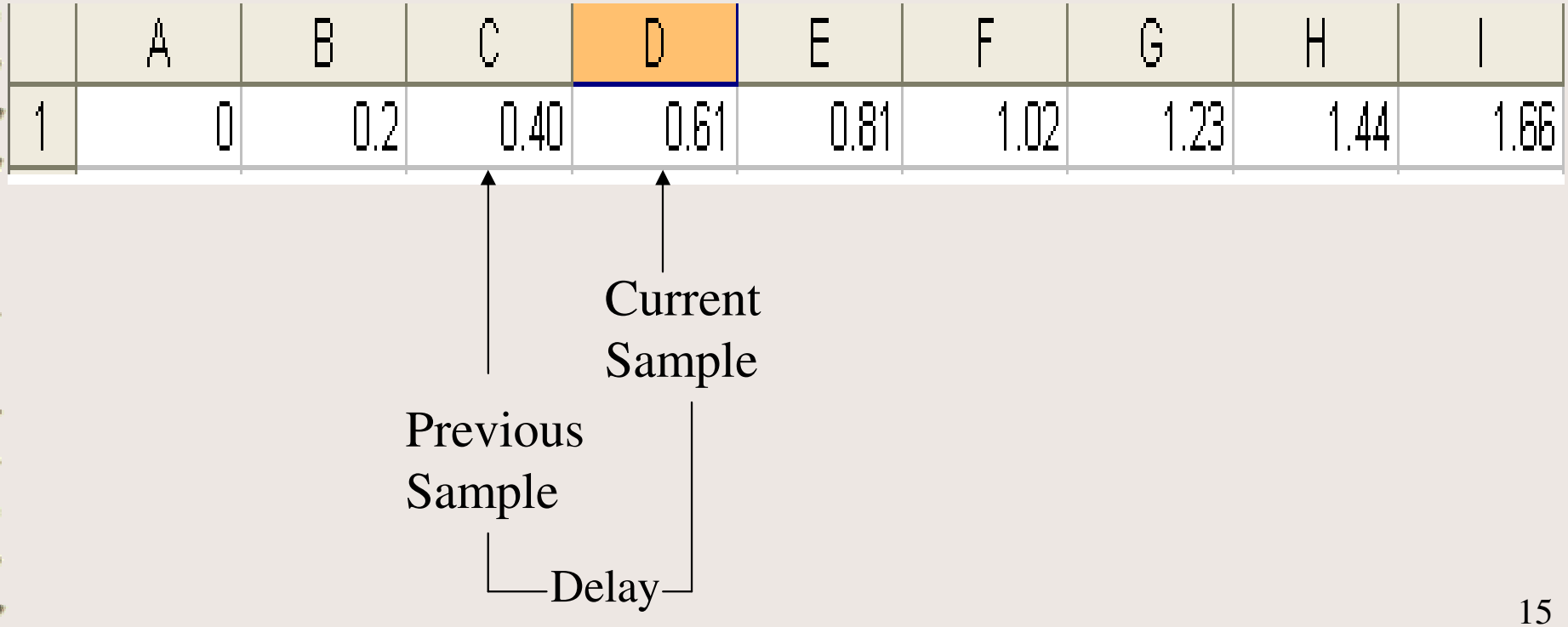
- Signal Generator – I & Q
  - Q = sin(x) I = cos(x)

	A	B	C	D	E	F	G	H	I	J
1	phase	0	0.4	0.8	1.2	1.6	2	2.4	2.8	3.2
2	cos	1	0.921061	0.696707	0.362358	-0.0292	-0.41615	-0.73739	-0.94222	-0.99829
3	sin	0	0.389418	0.717356	0.932039	0.999574	0.909297	0.675463	0.334988	-0.05837



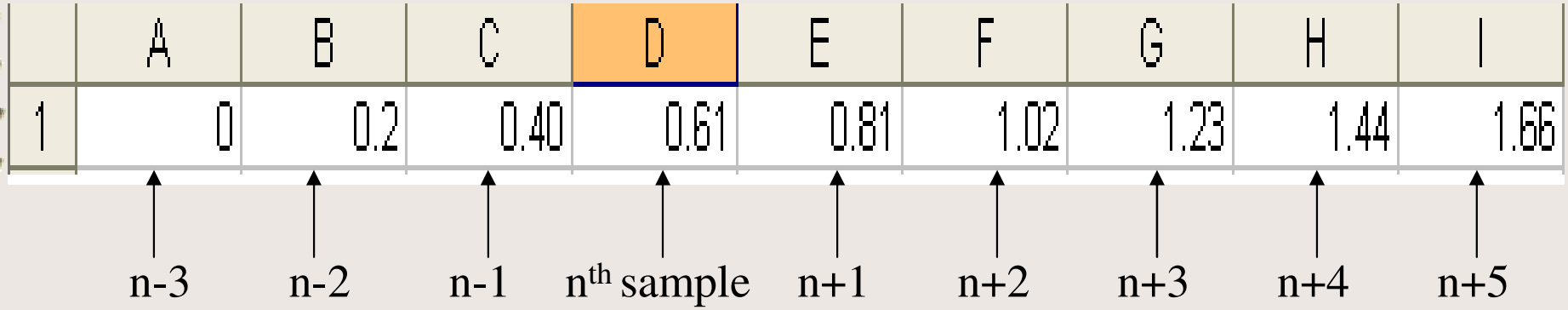
DSP Lab

- Digital Filters
  - Based on delays



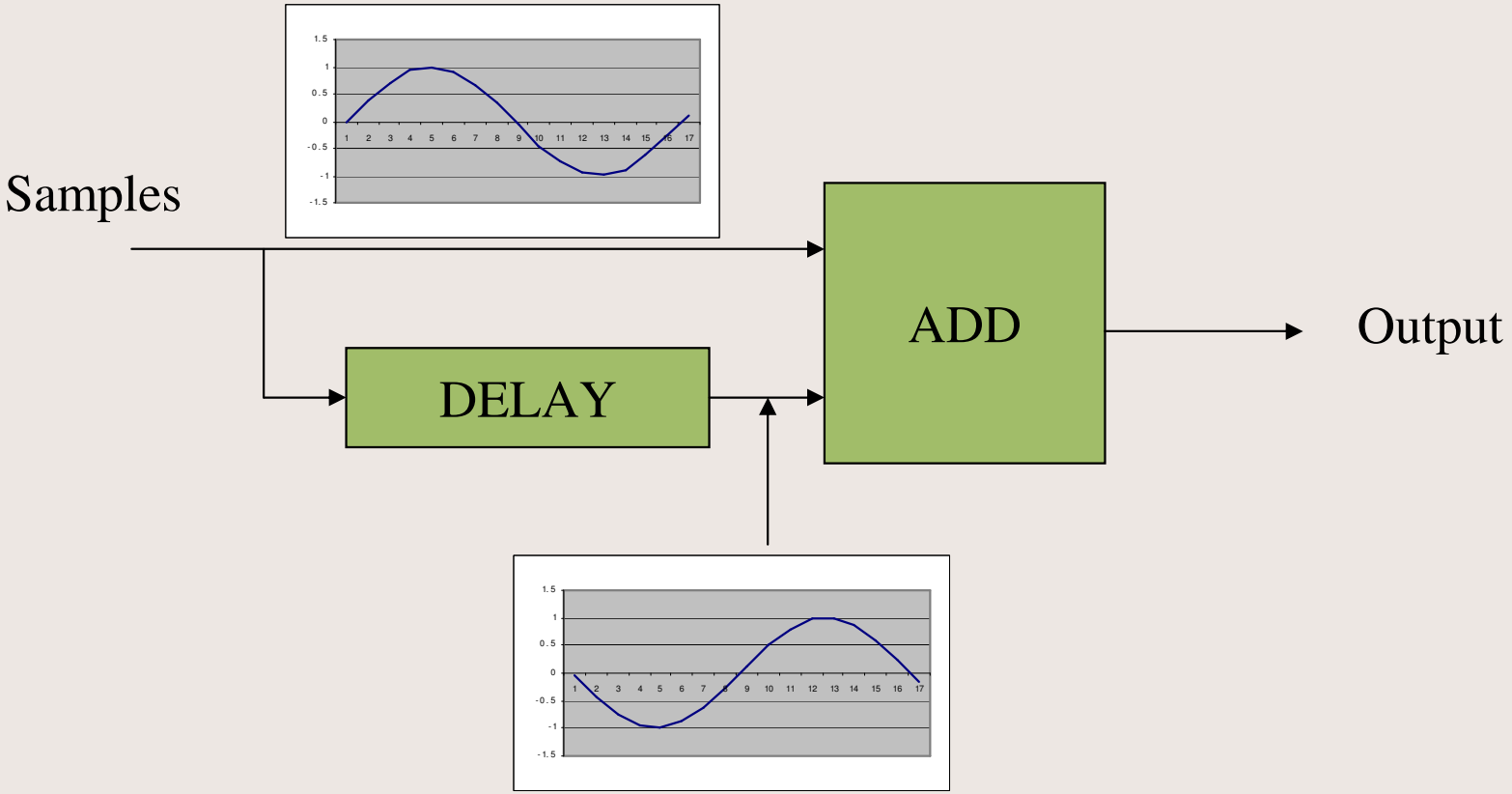
DSP Lab

- Digital Filters
  - Based on delays



DSP Lab

- Digital Filters
  - Based on delays
  - Simplest = Comb filter

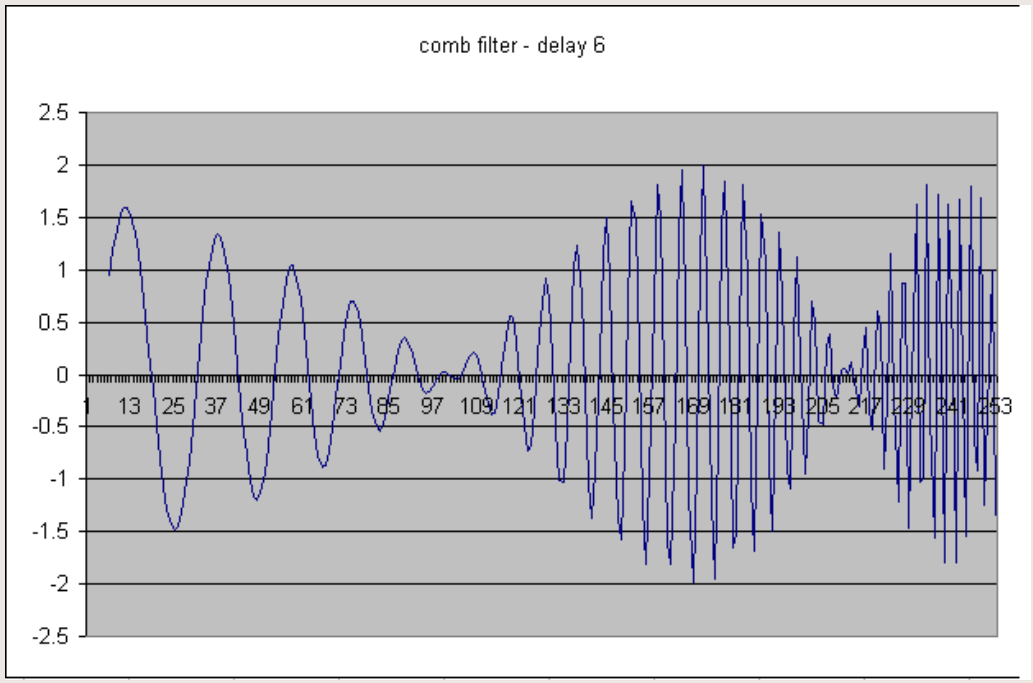


DSP Lab

- Comb Filter – delay = 6

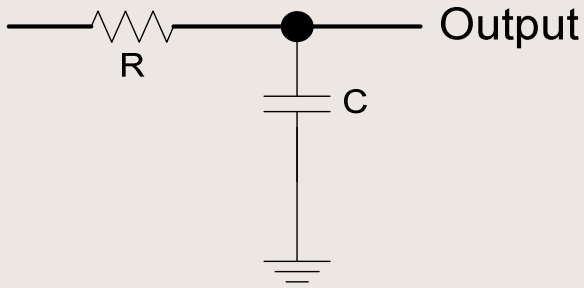
	A	B	C	D	E	F	G	H	I	J
1	phase	0	0.2	0.40	0.61	0.81	1.02	1.23	1.44	1.66
2	sin	0.00	0.20	0.39	0.57	0.73	0.85	0.94	0.99	1.00
3	comb filter - delay 6							0.94	1.19	1.39

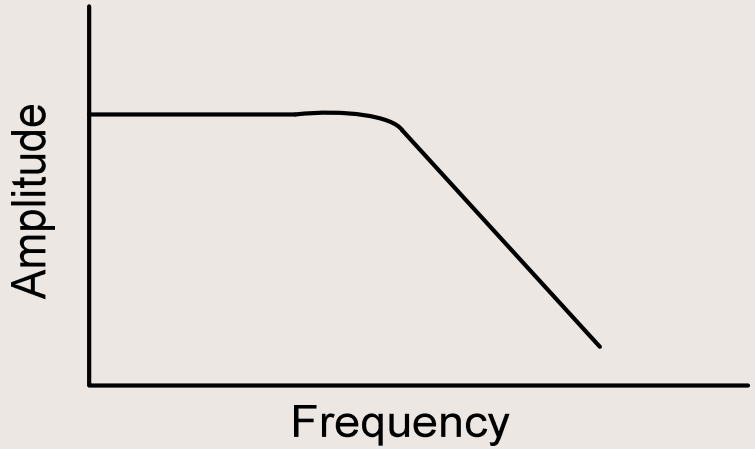
Sweep Generator



DSP Lab

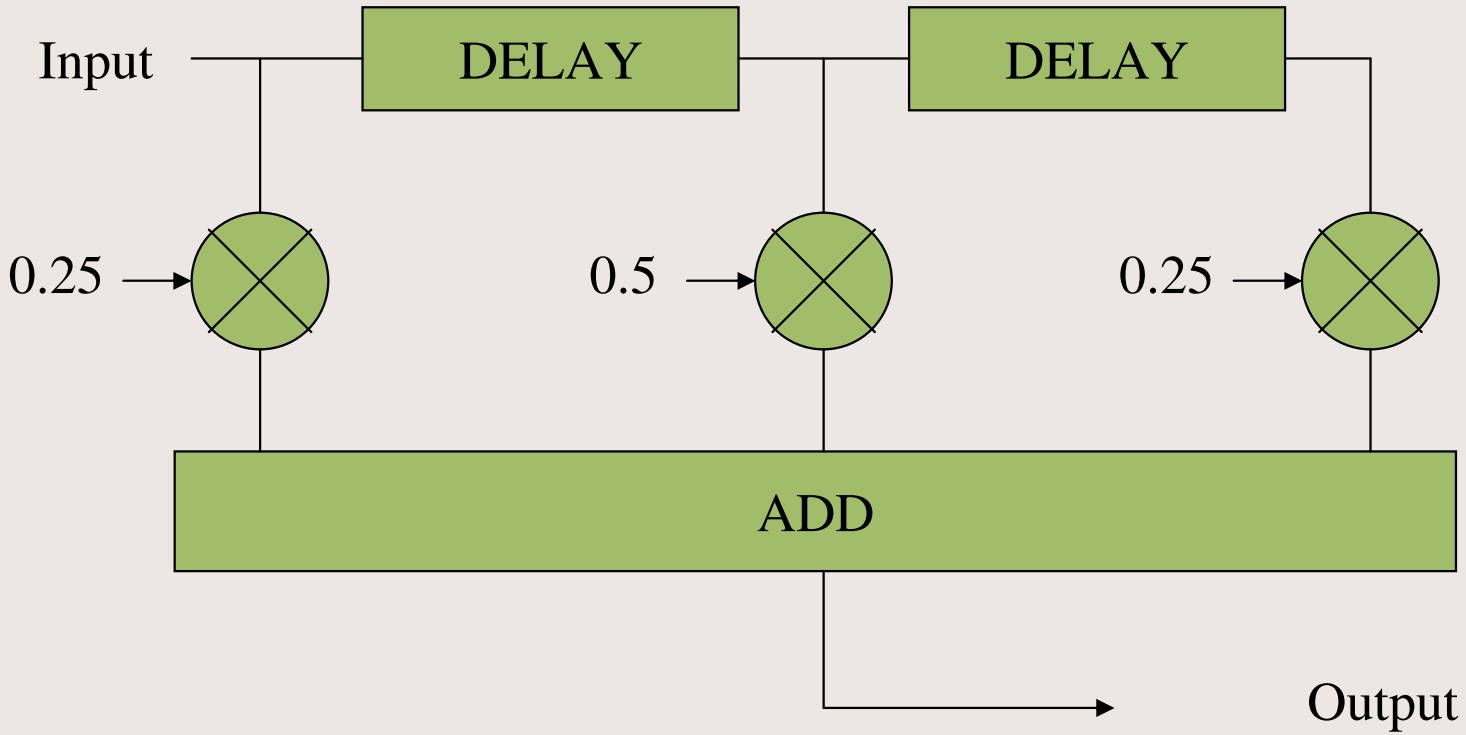
- Lowpass Filter





DSP Lab

- Lowpass Filter - FIR



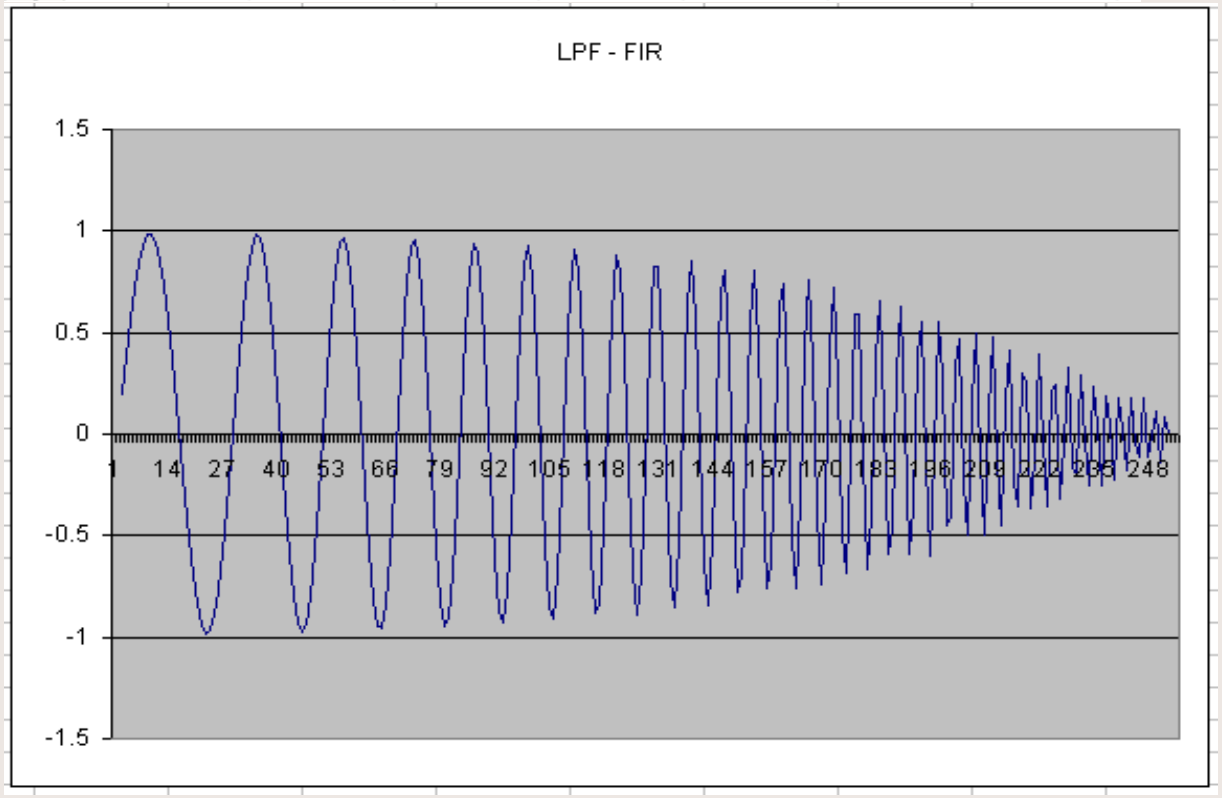
DSP Lab

- Lowpass Filter - FIR

D3 | =(0.25*D2)+ (0.5*C2)+ (0.25*B2)

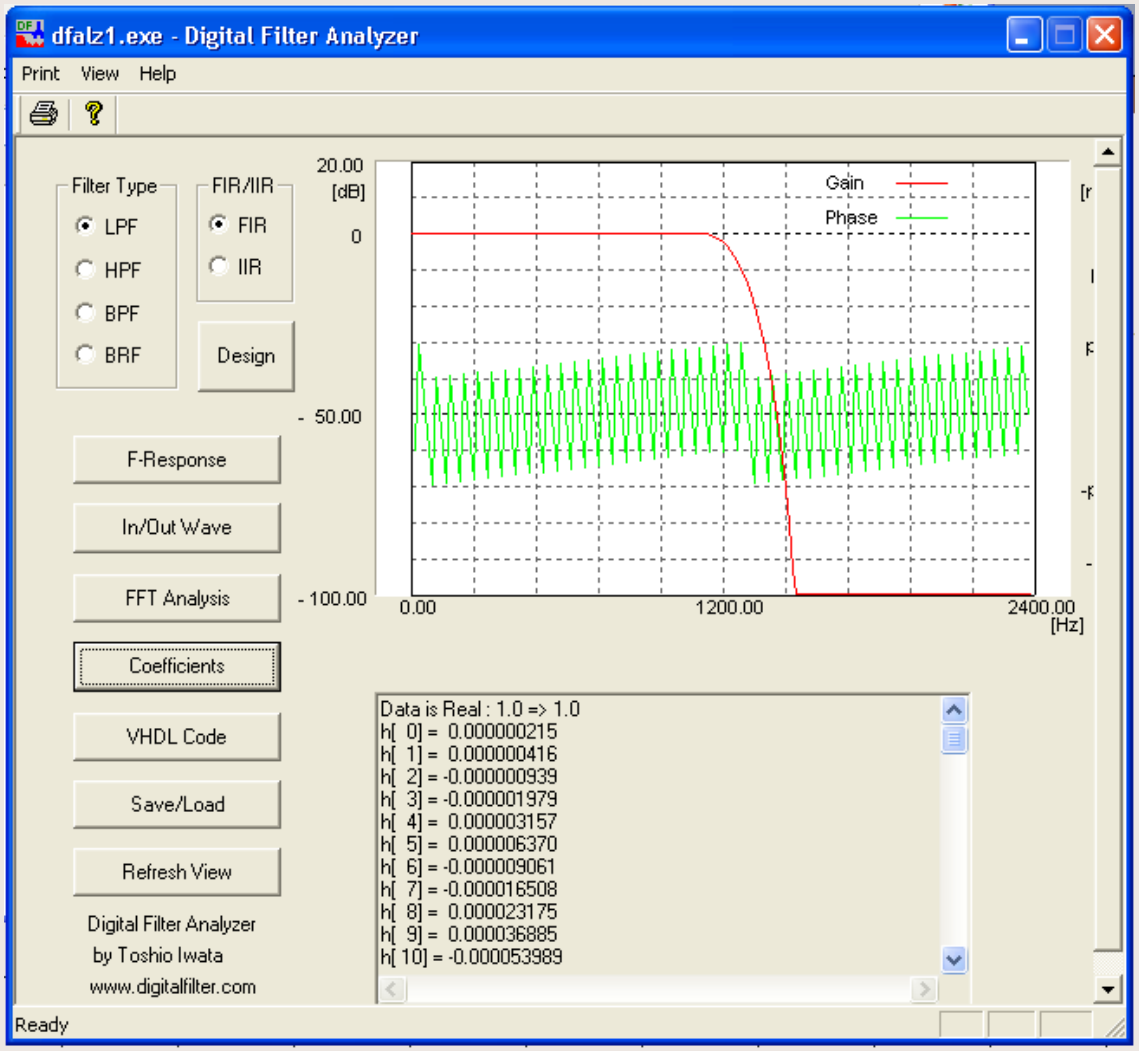
	A	B	C	D	E	F	G
1	phase	0	0.2	0.4	0.61	0.81	1.02
2	sin	0	0.2	0.39	0.57	0.73	0.85
3	LPF - FIR			0.1975	0.3875	0.565	0.72

Sweep Generator



DSP Lab

- Filter Coefficients

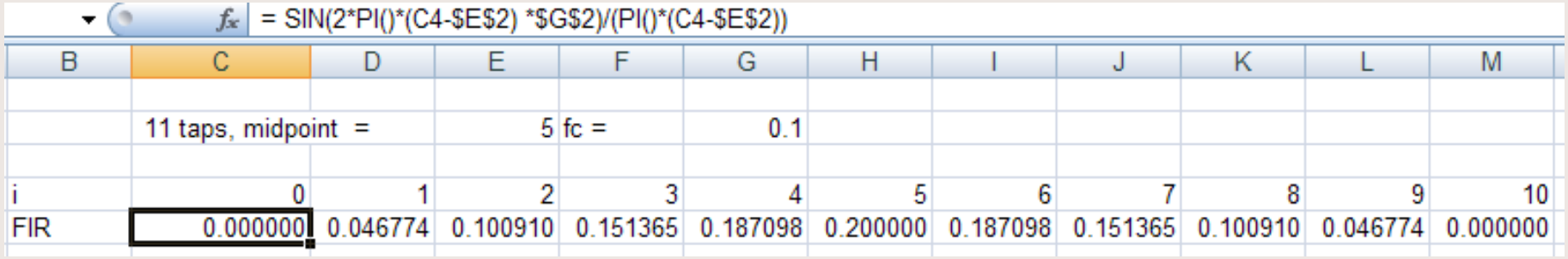


FIR Filter

- Variable frequency FIR Filter
- Formula to calculate tap values for a LPF

Tap value = sin[(2. π.(tap# - midtap#). Cutoff_frequency/

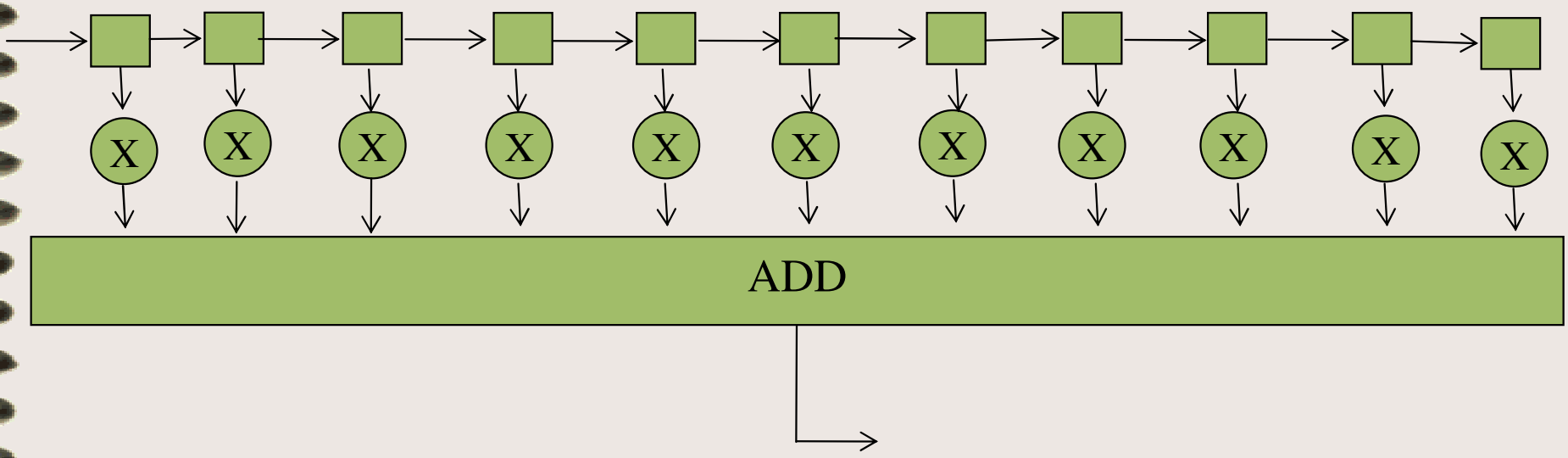
π.(tap# - midtap#)]



= SIN(2*PI()*(C4-E2) *G2)/(PI()*(C4-E2))

B	C	D	E	F	G	H	I	J	K	L	M
	11 taps, midpoint =		5	fc =	0.1						
i	0	1	2	3	4	5	6	7	8	9	10
FIR	0.000000	0.046774	0.100910	0.151365	0.187098	0.200000	0.187098	0.151365	0.100910	0.046774	0.000000

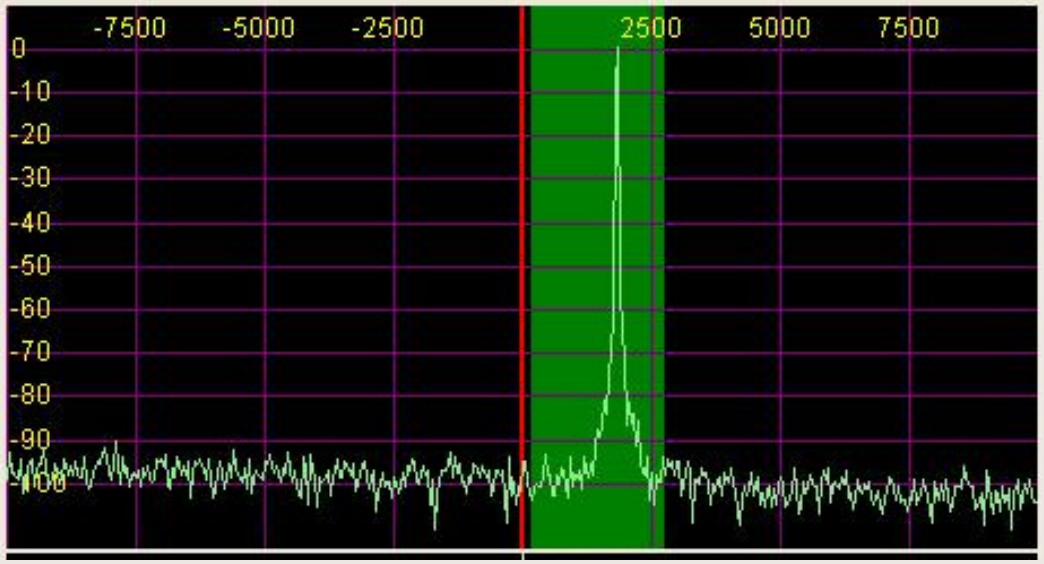
11 Tap FIR Filter



More Taps = Steeper roll off but higher latency

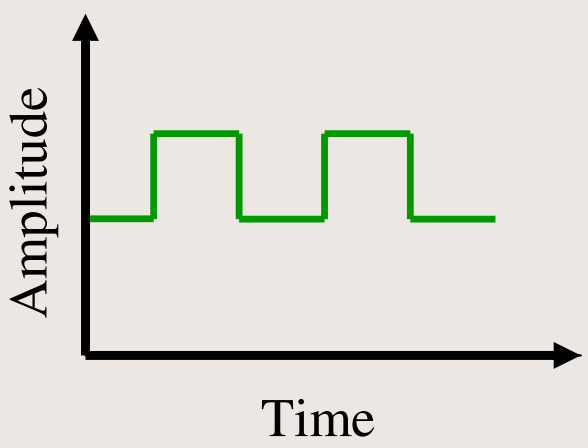
DSP Lab

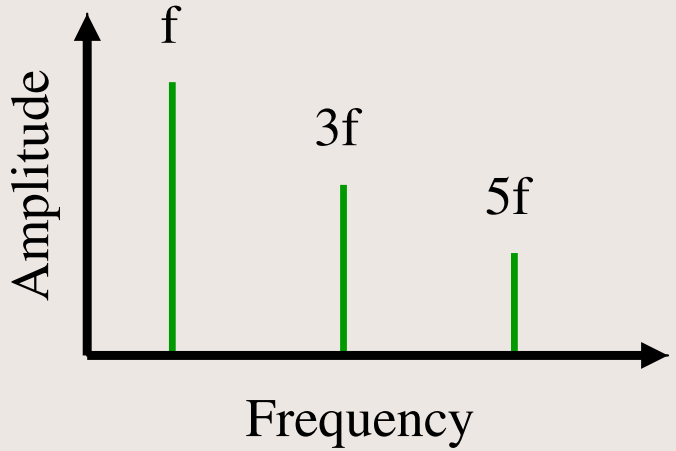
- Spectrum Analyzer
  - The basis of a Bandscope
  - Uses a ‘Fourier Transform’



DSP Lab

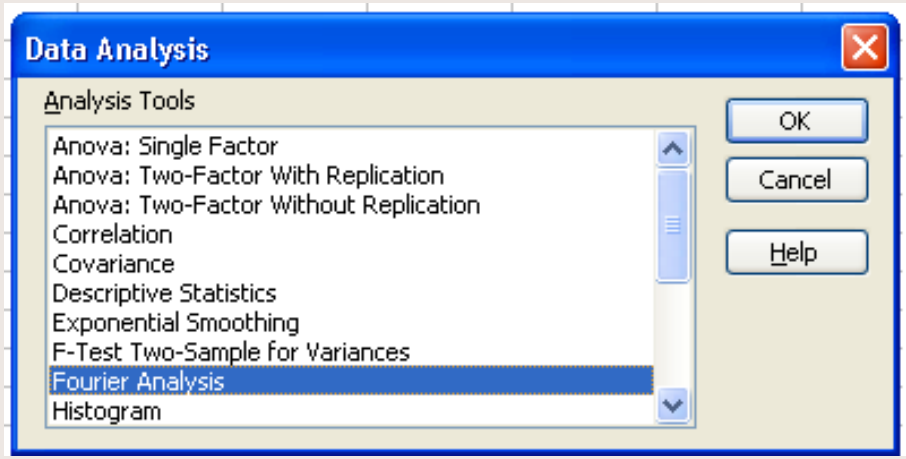
- Spectrum Analyzer – Fourier Transform
  - Converts between time and frequency domains





DSP Lab

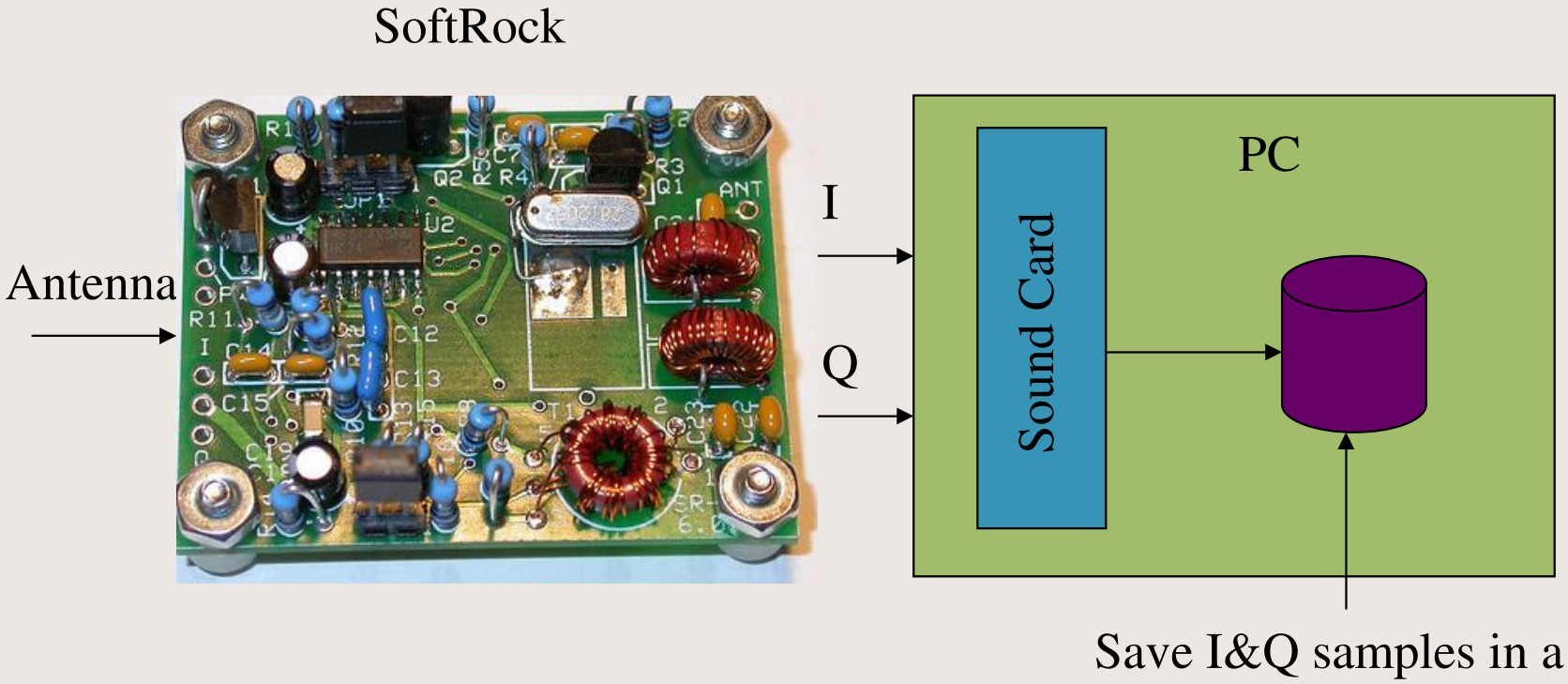
- Spectrum Analyzer – Fourier Transform
  - Could code ourselves
  - Already built into Excel!*
  - Tools > Data Analysis > Fourier Analysis



* May need to install – Tools>Add-Ins>Analysis ToolPak-VBA

DSP Lab

- Spectrum Analyzer
  - Capture ‘real’ data from SDR hardware

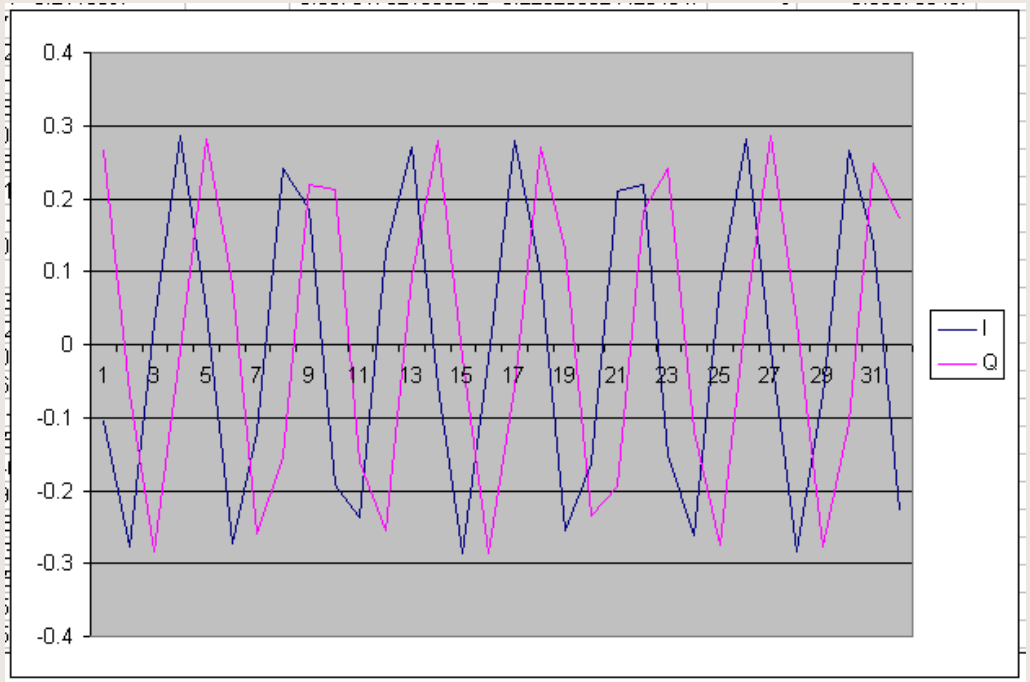


DSP Lab

- SoftRock I&Q data

	A	B	C
1			
2	Index	I	Q
3	0	-0.10456	0.265938
4	1	-0.27775	-0.06797
5	2	0.029969	-0.2844
6	3	0.285531	-0.00845
7	4	0.046419	0.281716
8	5	-0.27329	0.083743
9	6	-0.11991	-0.25959
10	7	0.240913	-0.15363

4090	4087	-0.11225	-0.26298
4091	4088	0.245338	-0.14646
4092	4089	0.17777	0.223548
4093	4090	-0.198	0.206122
4094	4091	-0.23103	-0.16862
4095	4092	0.136021	-0.25147
4096	4093	0.26719	0.101138
4097	4094	-0.06467	0.278268
4098	4095	-0.28471	-0.02686



DSP Lab

- Spectrum Analyzer
  - Convert data to complex form

D2 fx =+COMPLEX(B2,C2)

	A	B	C	D
1	Index	I	Q	complex(I,q)
2	0	-0.10456	0.265938	-0.104556+0.265938i

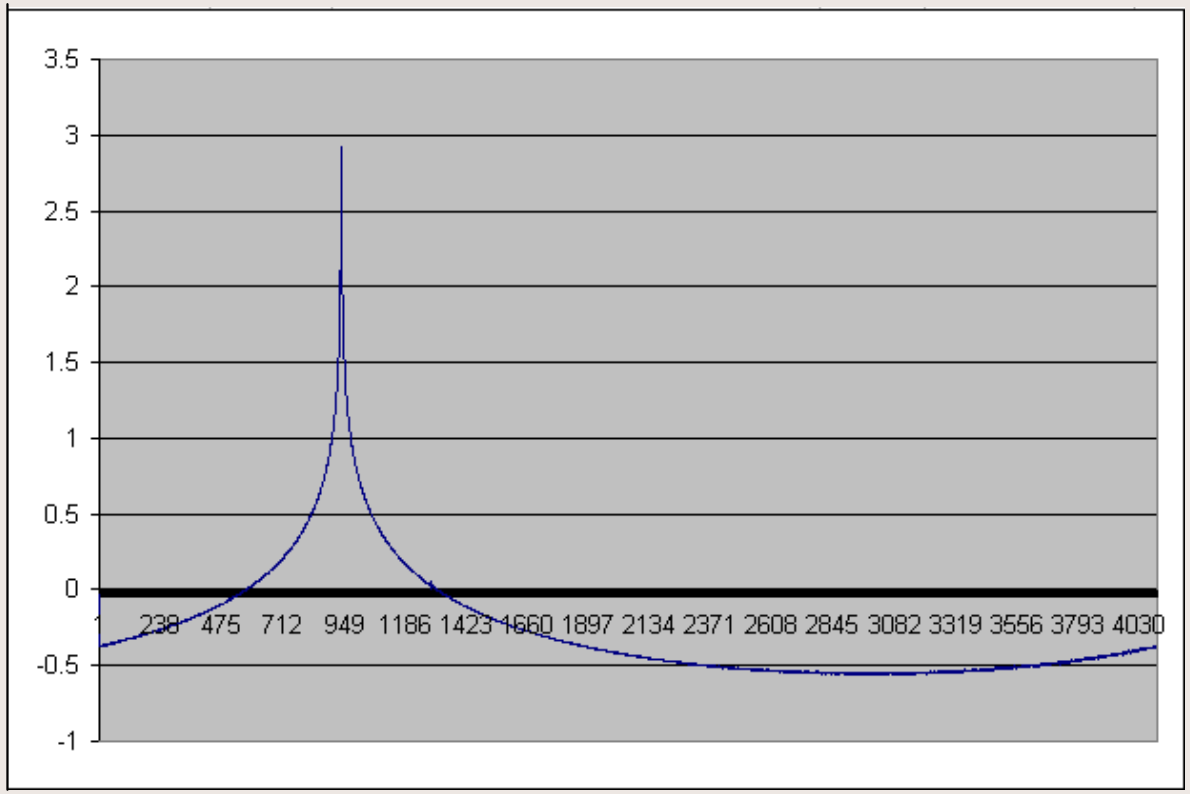
  - Apply Fourier Transform
  - Convert to magnitude and take $\log_{10}$ of result

F2 fx =LOG(+IMABS(E2),10)

	E	F
1	fft(i,q)	log10 (mag(fft))
2	-0.877055000000003-0.301133999999998i	-0.032774218

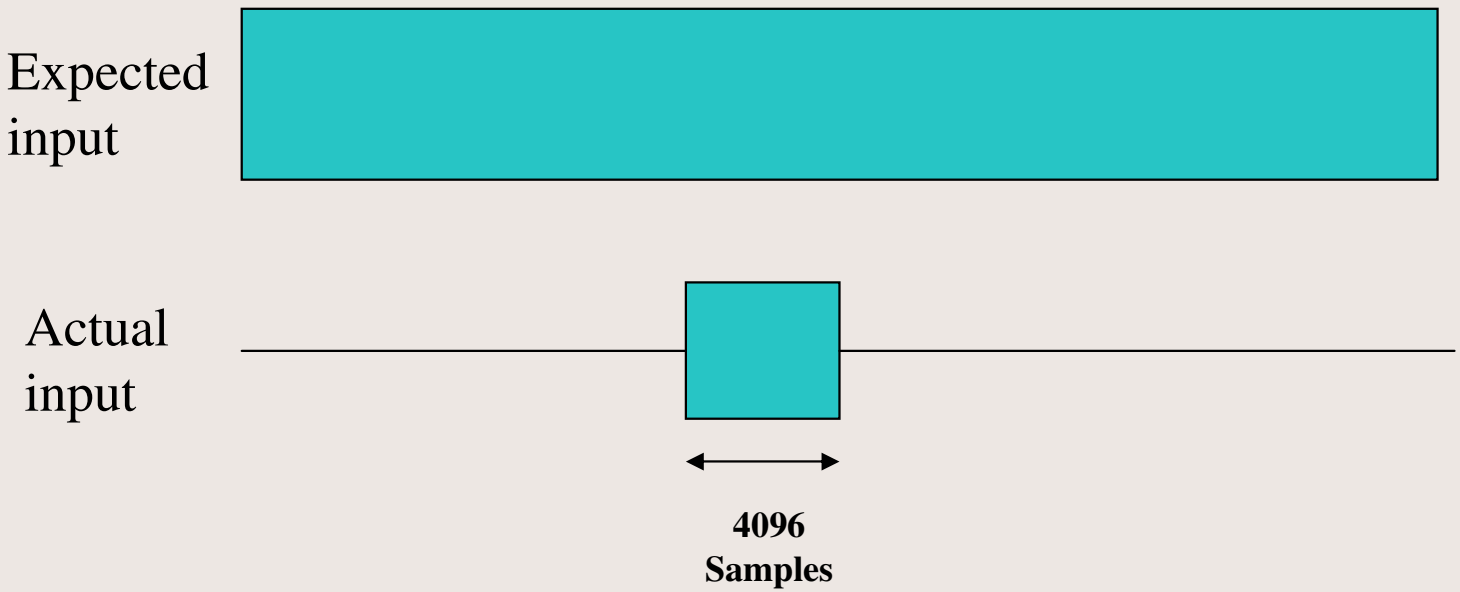
DSP Lab

- Spectrum Analyzer



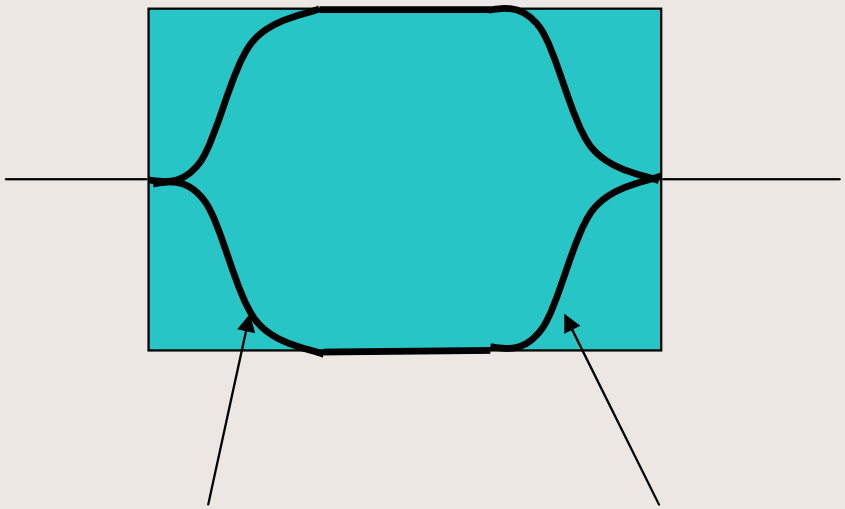
DSP Lab

- Spectrum Analyzer



DSP Lab

- Spectrum Analyzer



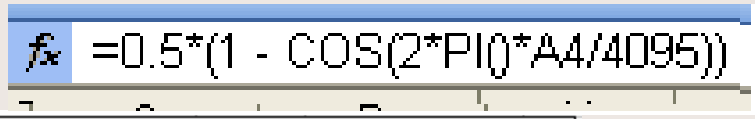
DSP Lab

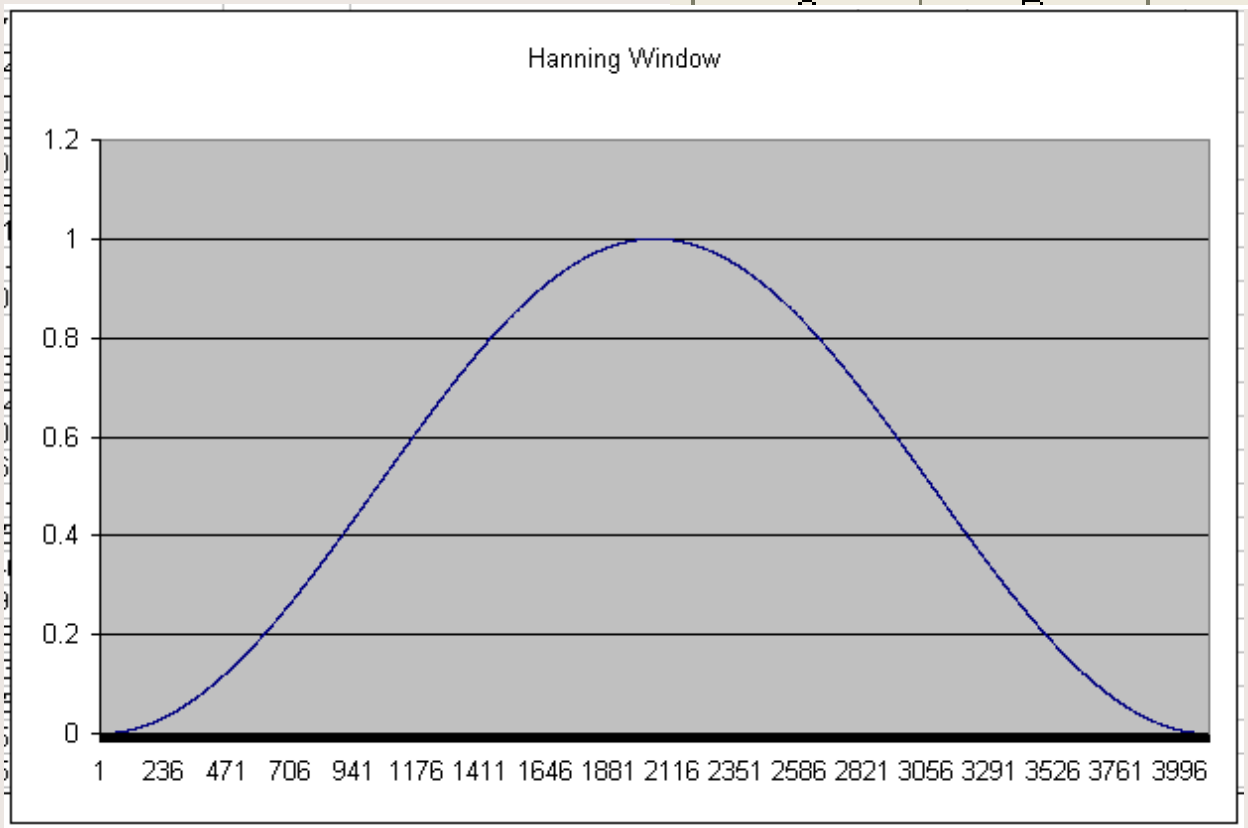
- Spectrum Analyzer – Window Functions

Window Function	Magnitude Resolution	Frequency Resolution
Rectangle	Very Low	Very High
Hanning	High	Low
Hamming	Normal	Normal
Blackman	High	Low
Blackman -Harris	Very High	Very Low
Bartlett	Low	High

DSP Lab

- Spectrum Analyzer – Window Functions
  - Hanning (after Julius von Hann)
  - $0.5(1 - \cos(2\pi i/N-1))$



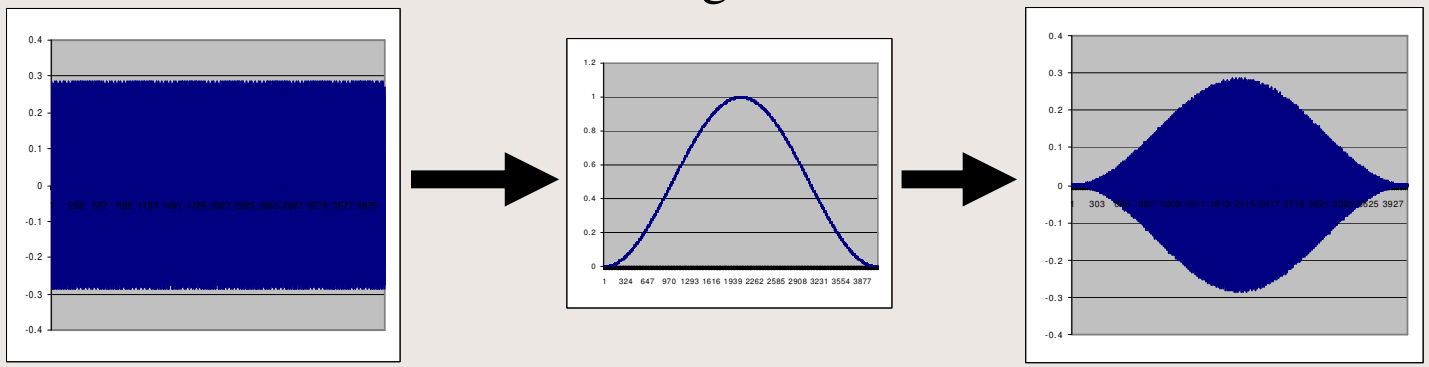


DSP Lab

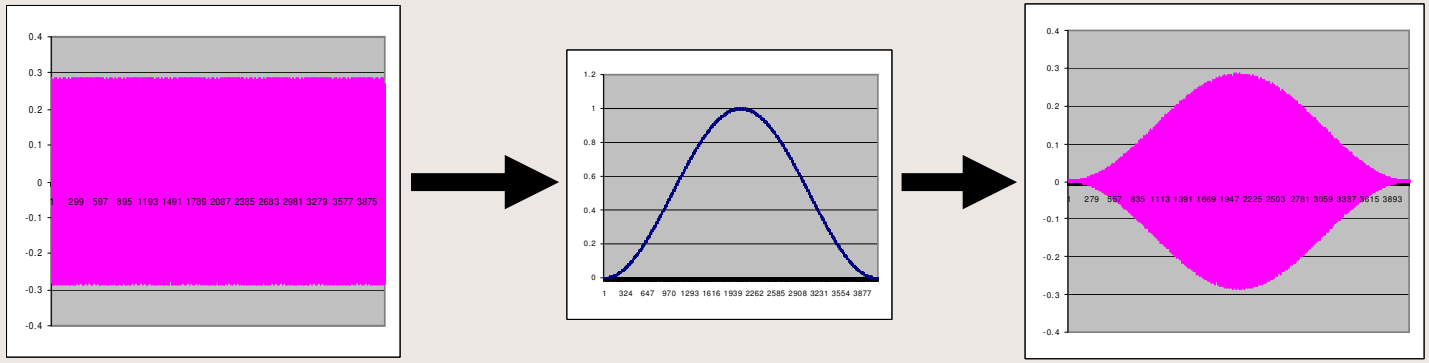
- Spectrum Analyzer – Window Functions

Hanning Window

I

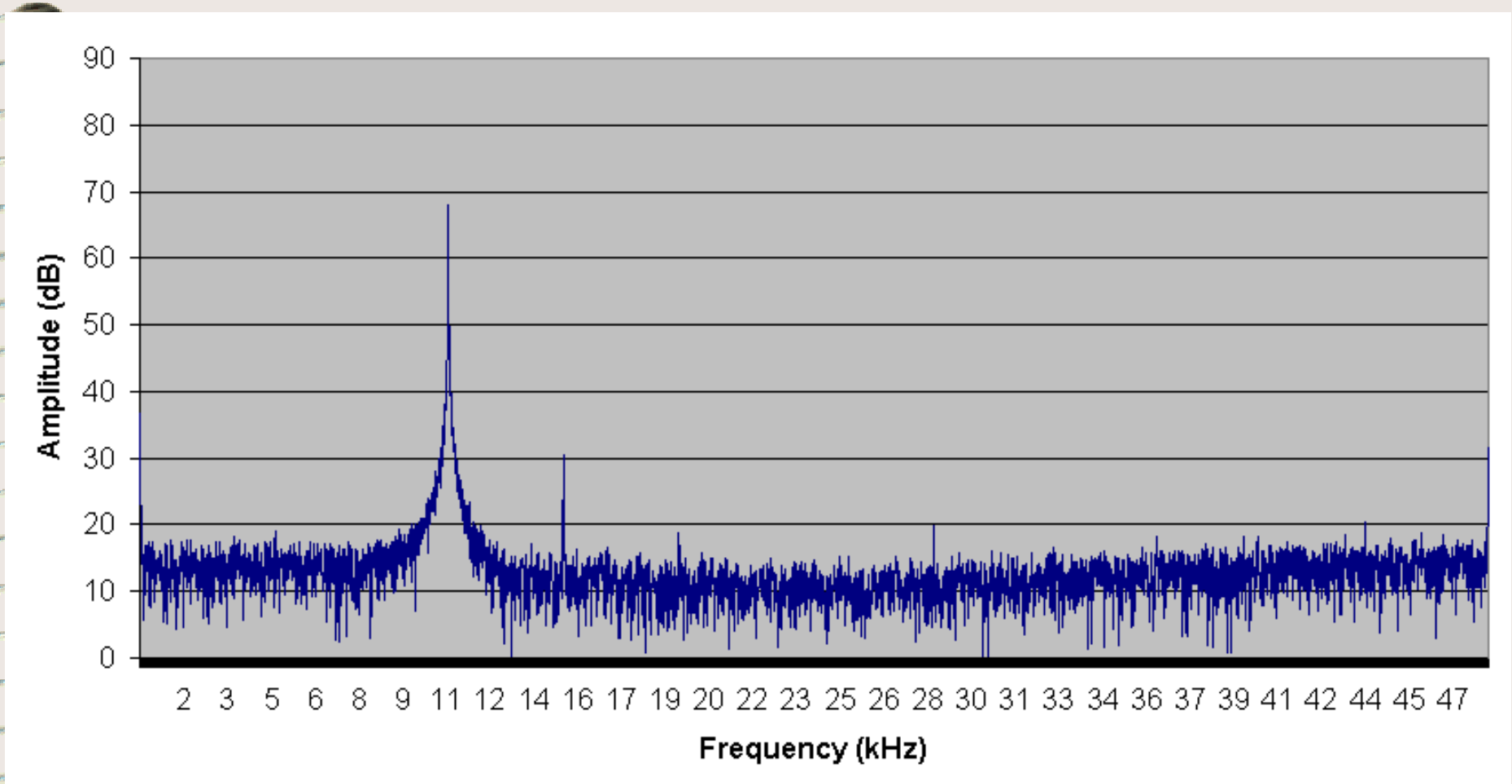


Q



DSP Lab

- Spectrum Analyzer



DSP Lab

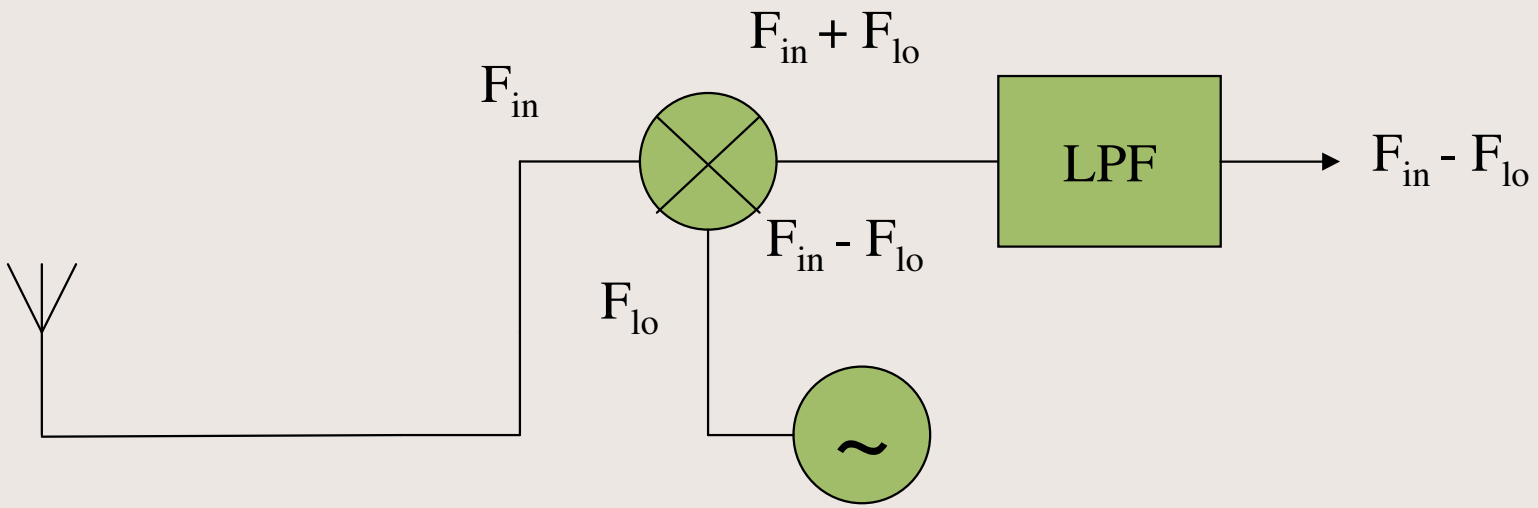
- Summary – by using a spread sheet we can:
  - build DSP test gear
  - investigate DSP filters
  - look at real samples from SDR hardware
  - "learn by doing"
  - www.scilab.org
  - www.digitalfilter.com
  - Presentation and files at www.hamsdr.com

Part II - DSP Applied to SDR

- The fundamental building block of a phasing receiver is the direct conversion receiver.
- Let's analyze how this works

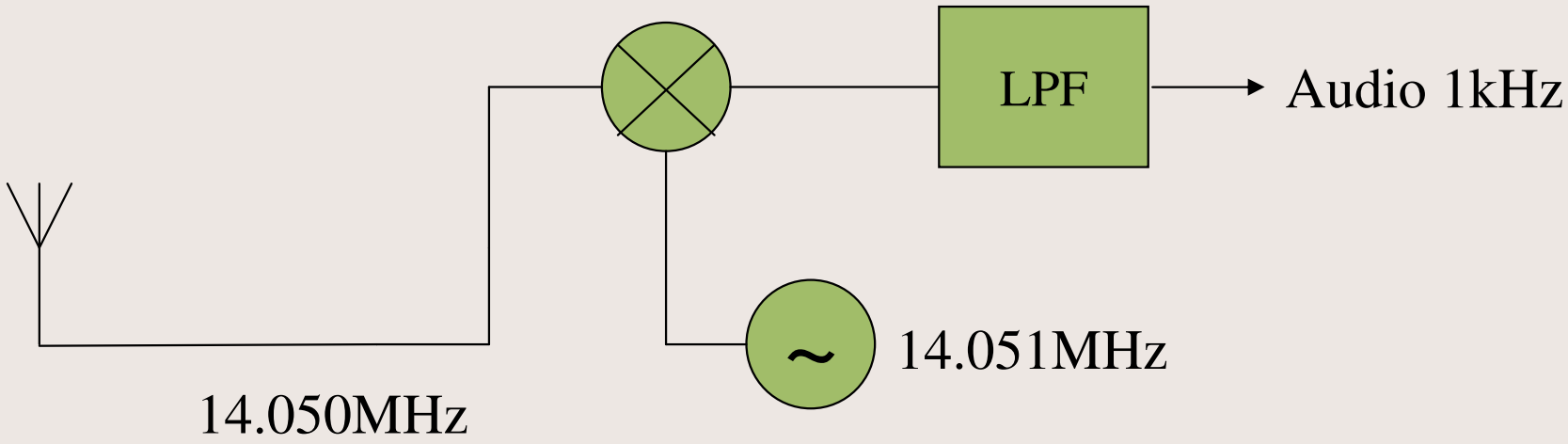
Block Diagram

- Based on Direct Conversion radio



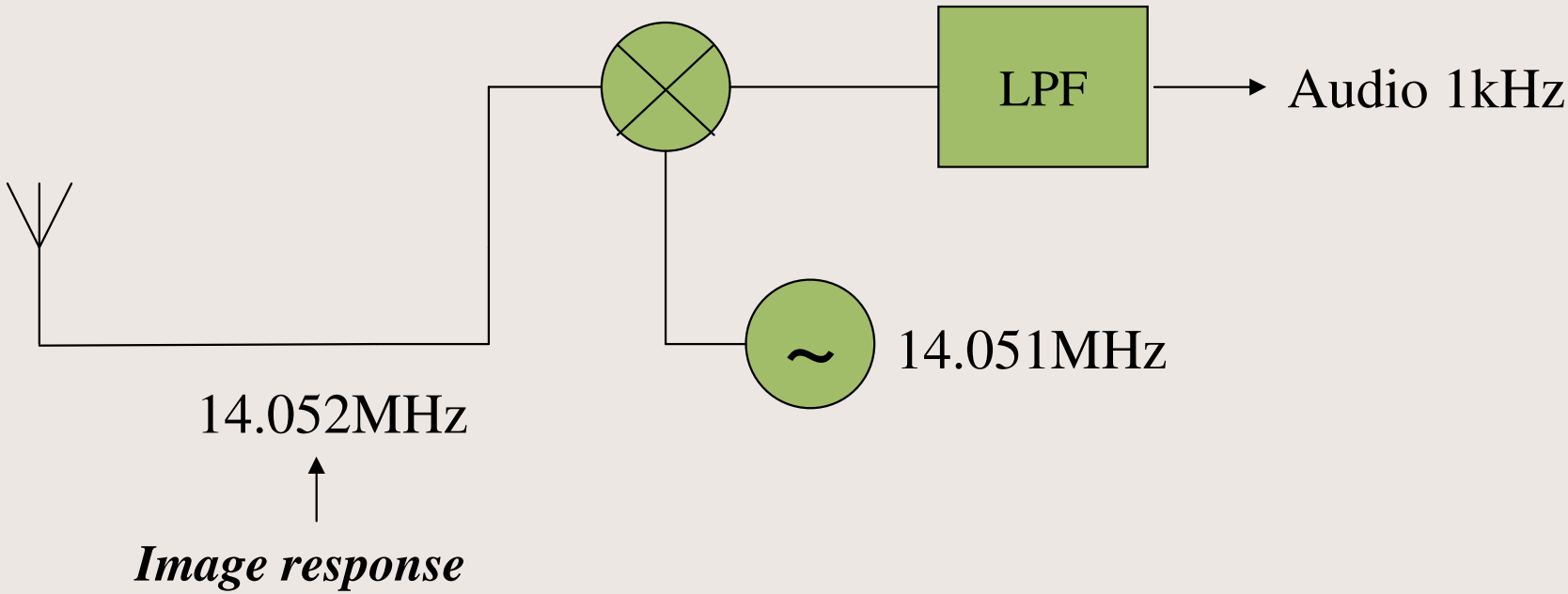
Block Diagram

- Based on Direct Conversion radio



Block Diagram

- Based on Direct Conversion radio

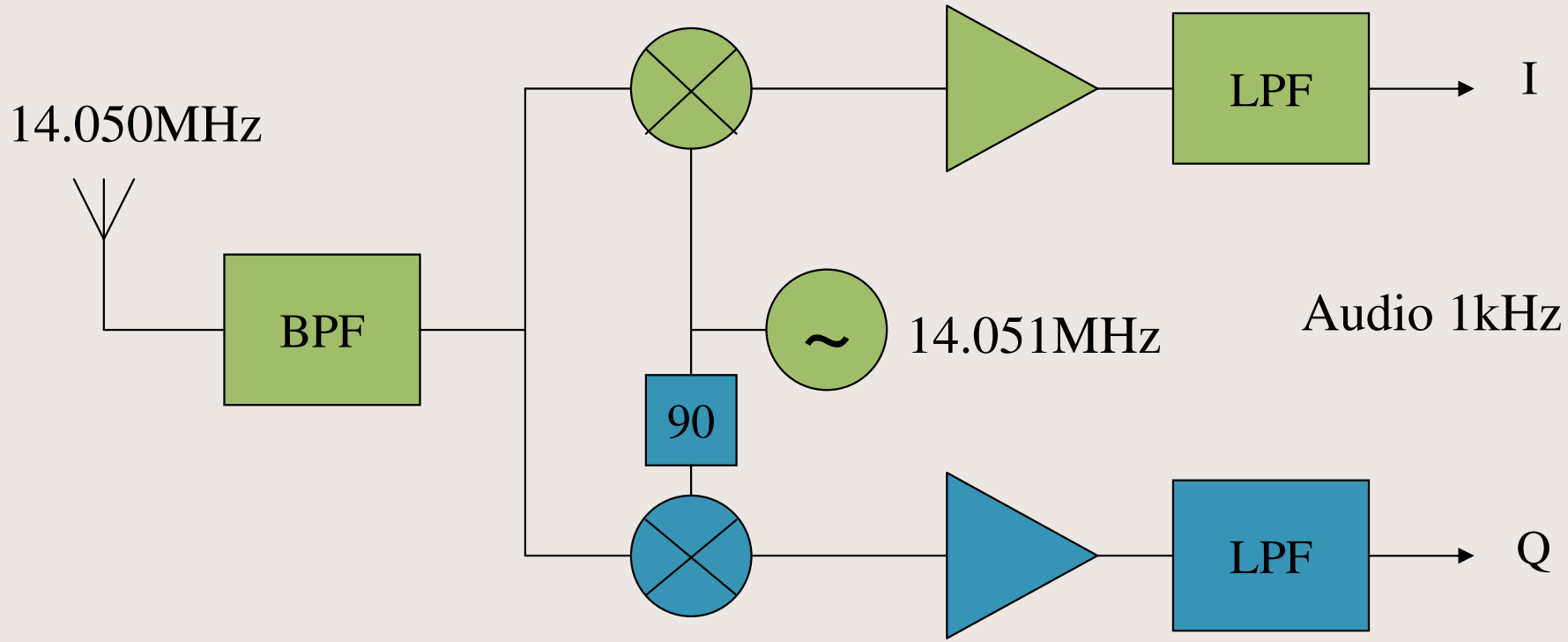


Direct Conversion Issues

- Image response
- Radiation of Lo from antenna socket
- Mains ‘hum’ on incoming signals
- Instability – high AF stage gain
- MW broadcast station breakthrough
- Hand capacitance effects
- Can be solved using analogue techniques ! (Heathkit HW -7/8/9)
- DSP techniques solve many of these issues

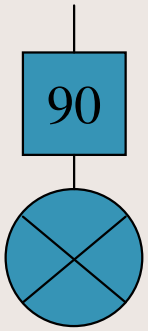
Block Diagram

- Direct conversion Phasing Receiver

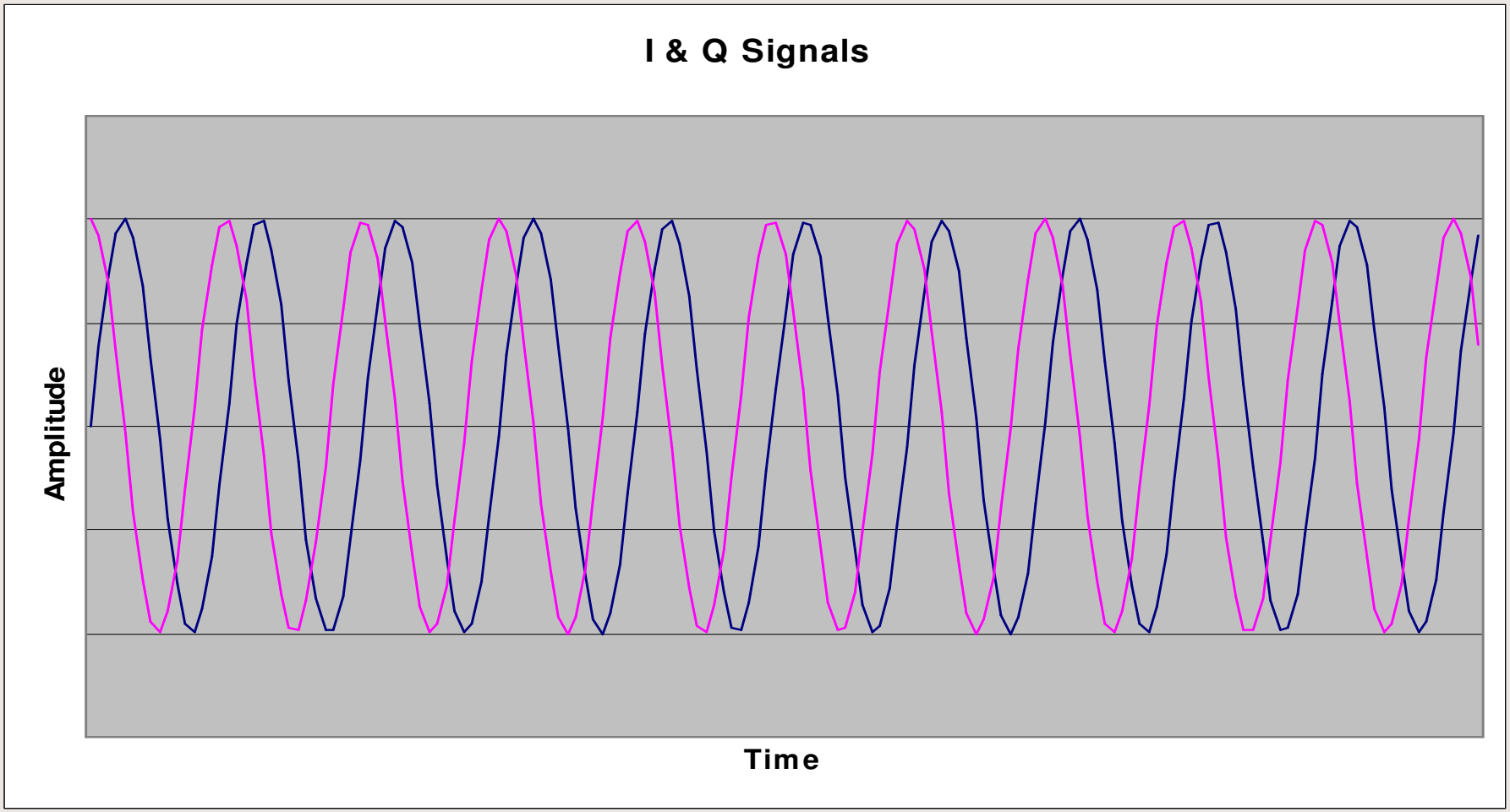


Removing the Image

- We now have two outputs, I & Q, that are identical – right?
- Not exactly! The 90 degree phase shift on the lower Lo signals shifts the phase of the Q output by 90 degrees



I & Q Signals



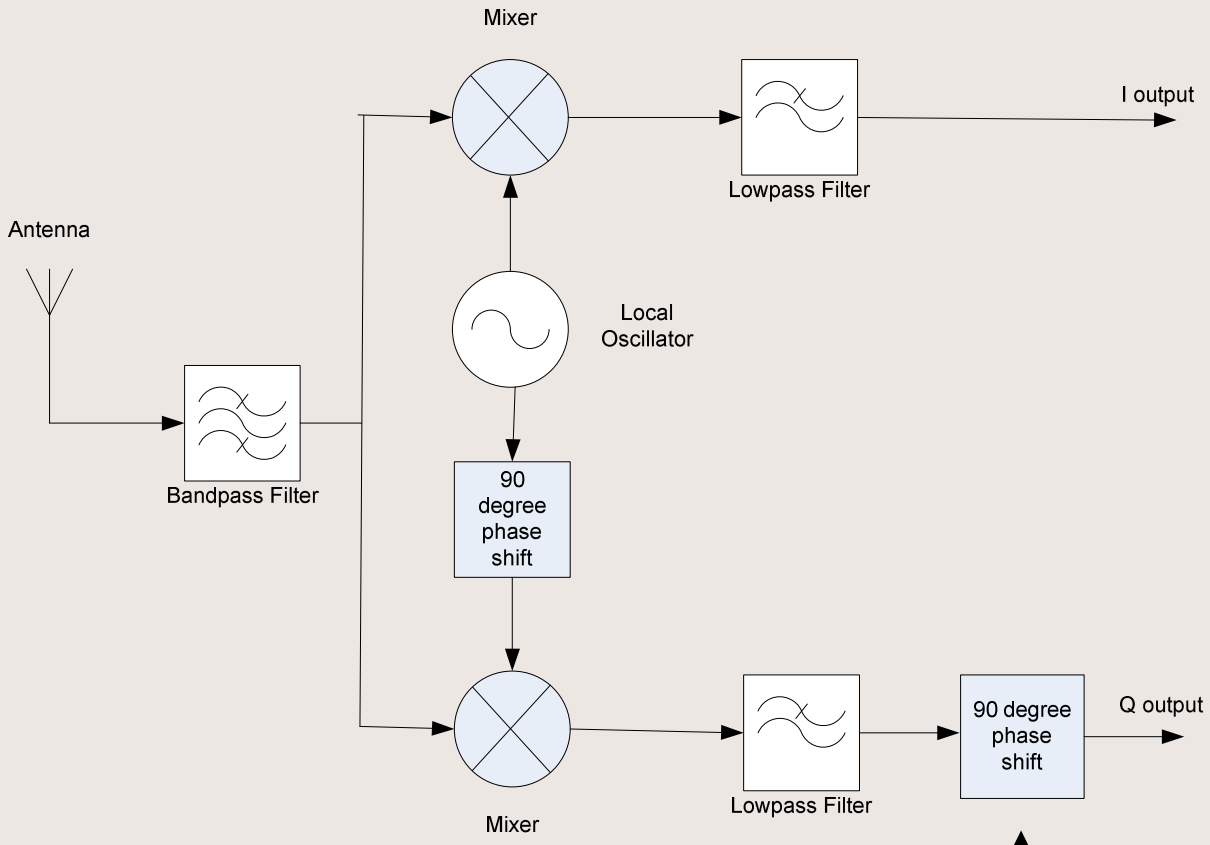
Why I & Q

- Why go to all the trouble to duplicate part of the radio?
- Because we can remove the image AND
- With I & Q we can demodulate ANY signal (AM, FM, SSB, CW, PSK, SSTV, FSK etc) or any FUTURE mode!
- How?
- Let's look at how the image is removed and how SSB and CW is demodulated.

I & Q Relationship

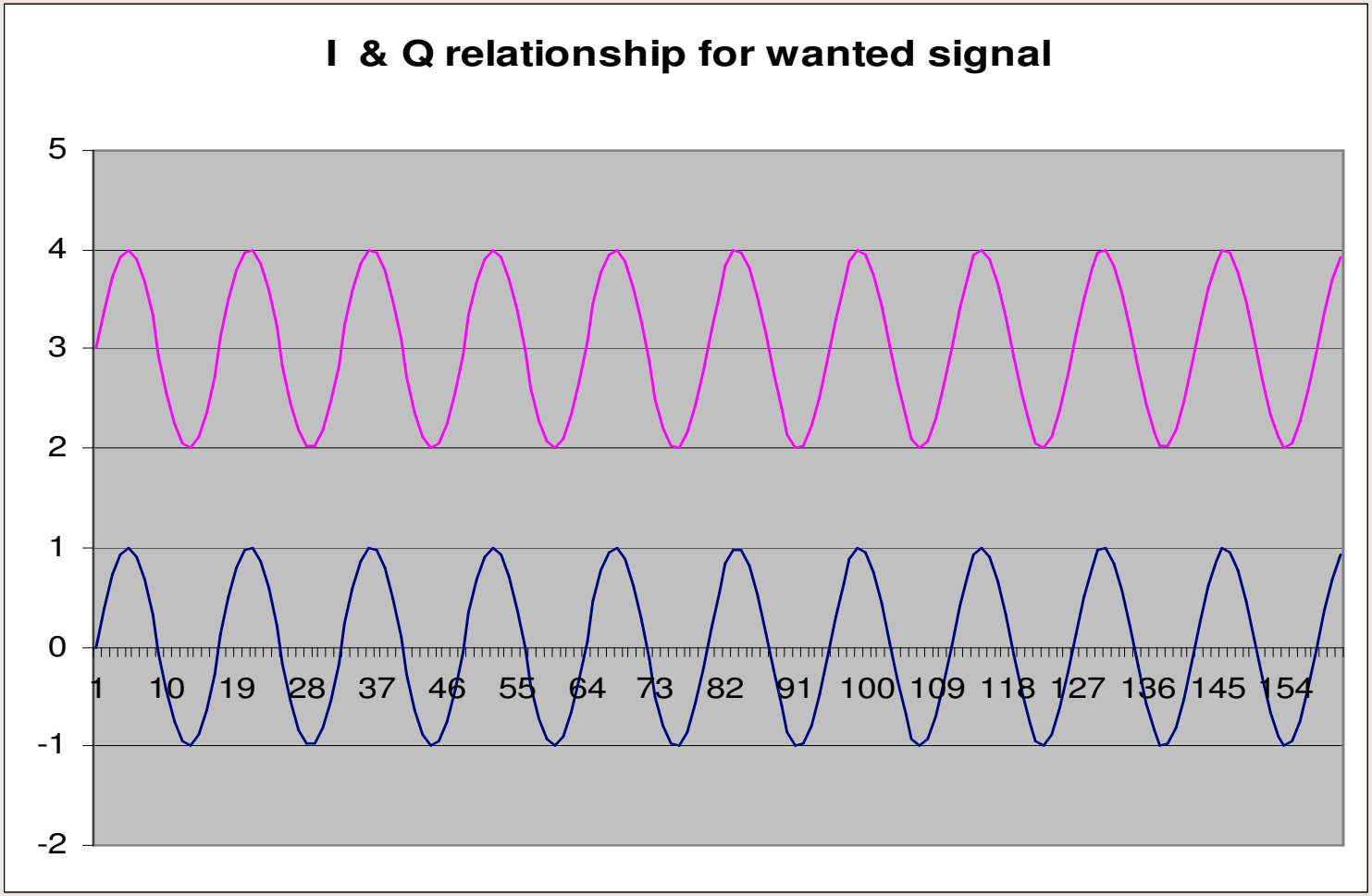
- **VERY IMPORTANT**
- For the wanted signal I leads Q
- For the image signal Q leads I

Image Removal

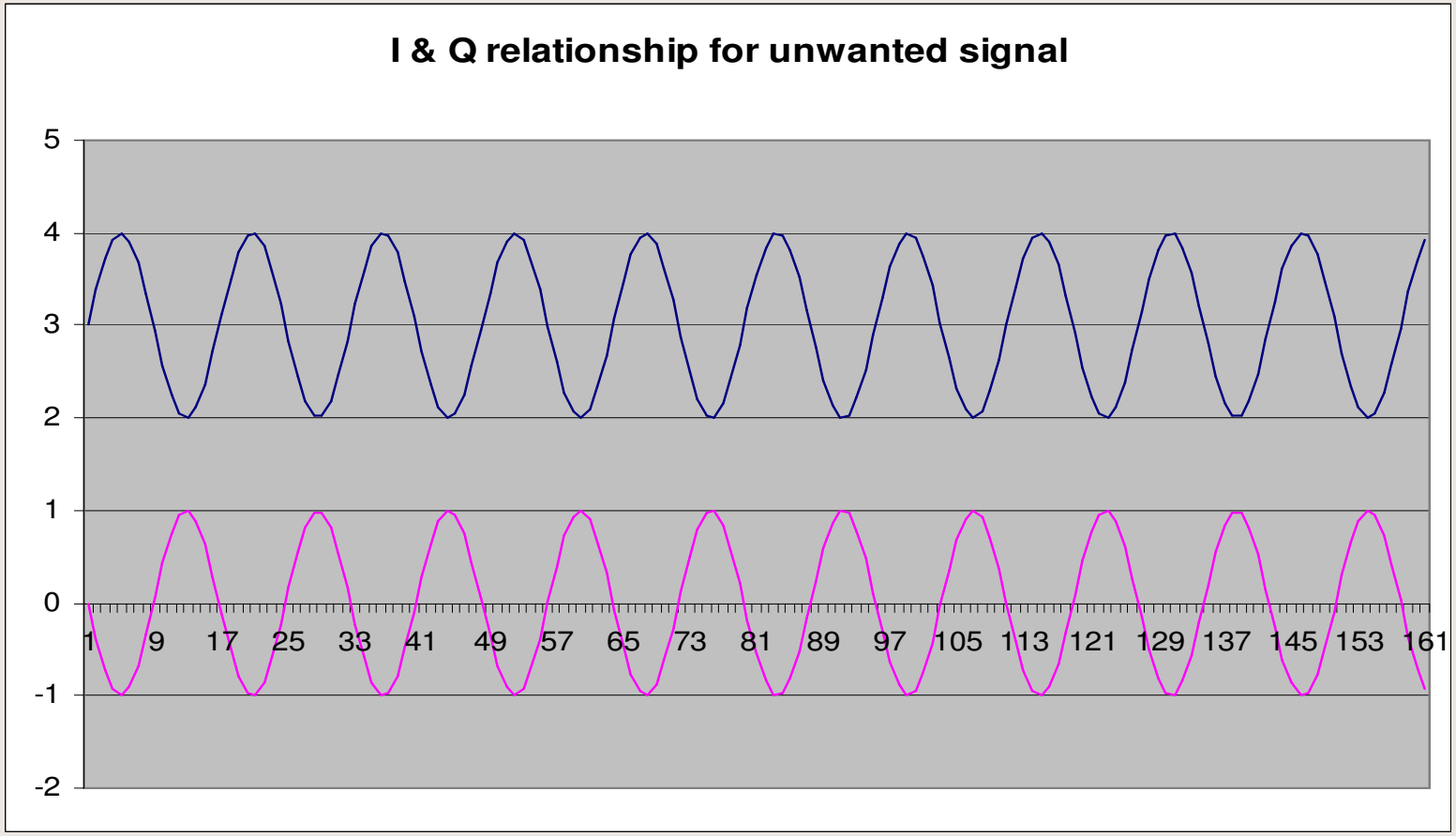


Add a 90 degree phase shift to the Q signal

I & Q – wanted signal



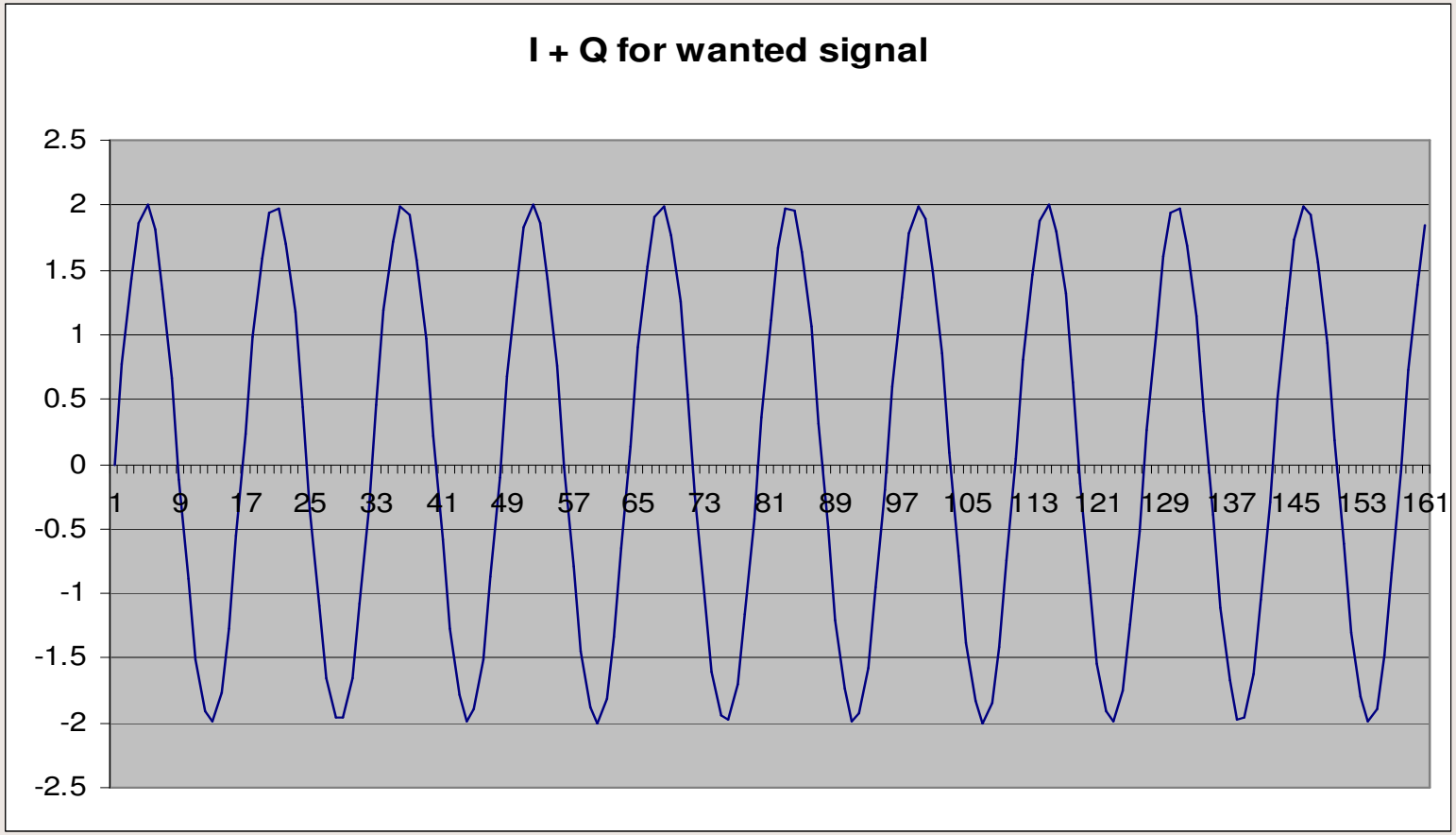
I & Q – image signal



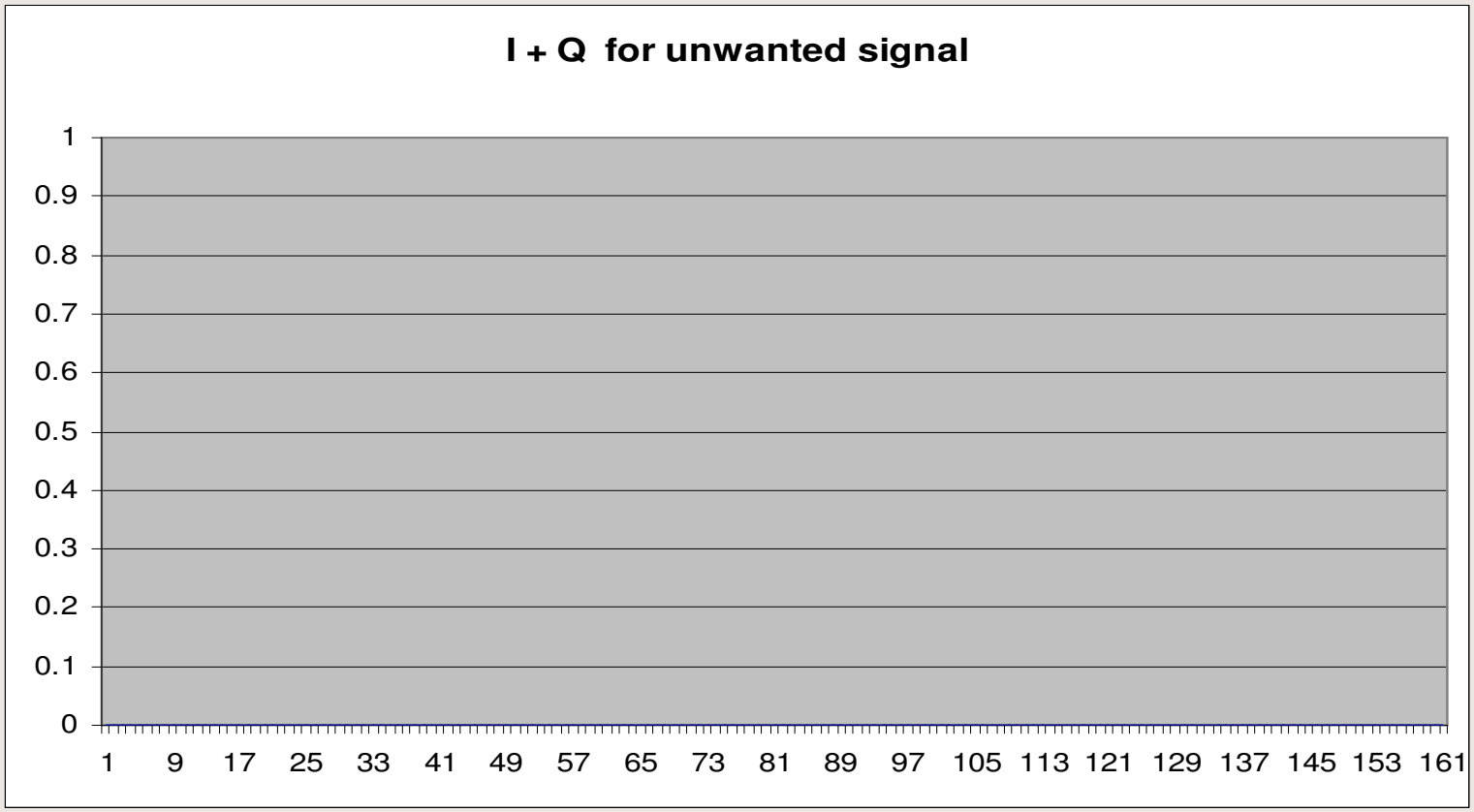
The Solution!

- If we add I & Q then we eliminate the image signal i.e. an LSB receiver
- If we subtract I & Q the we eliminate the wanted signal i.e. an USB receiver

Wanted Signal



Unwanted Image



All done?

- Not quite!
- The amount of image suppression depends on:
  - How close to 90 degrees phase we achieve
  - How close in amplitude I & Q are

I & Q Accuracy

- Image rejection Phase(deg) Amplitude(dB)

40dB	1	0.1
60dB	0.1	0.01
80dB	0.01	0.001
100dB	0.001	0.0001

- This accuracy must hold over each ham band and 300Hz-3kHz, with temperature, component aging, vibration, voltage etc

I & Q Accuracy

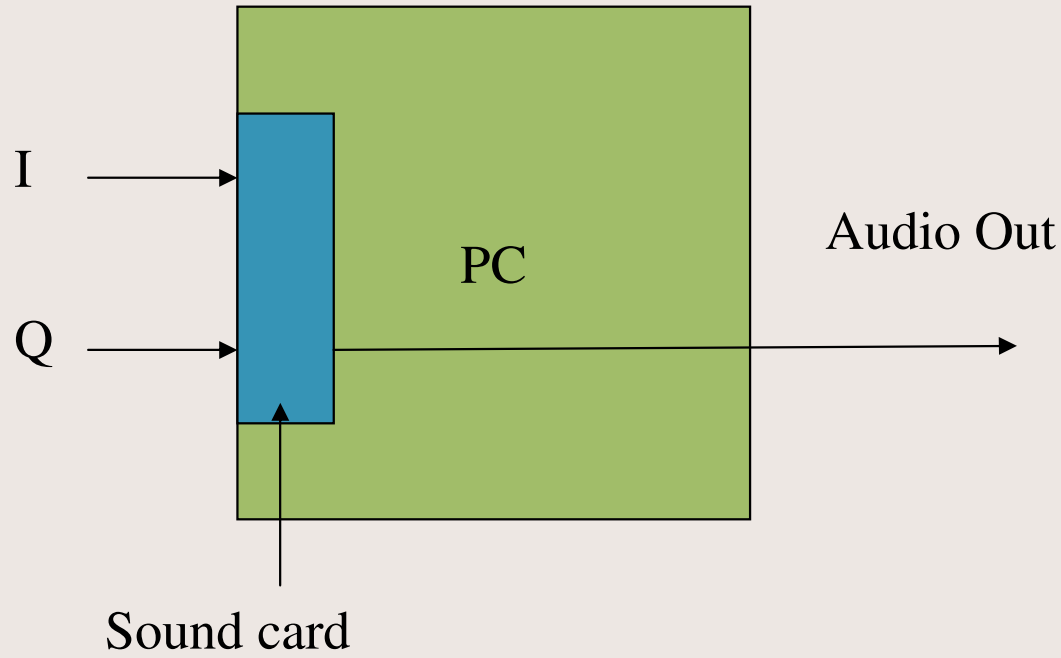
- The high phase and amplitude tolerances was the reason phasing techniques fell out of favor in analogue radios

DSP Applied to the problem

- What happens if we process the I&Q signals digitally?
- Digital Signal Processing:
  - Is not affected by temperature
  - Is not affected by component ageing
  - Is not affected by component tolerances
  - Does not require values to be ‘tweeked’
  - Is 100% reproducible
  - Can meet the I & Q tolerance requirements for 100db of image suppression

Software Defined Radio

- Digitize I&Q and use software to process
- Easiest way is to use a PC and a sound card



SDR

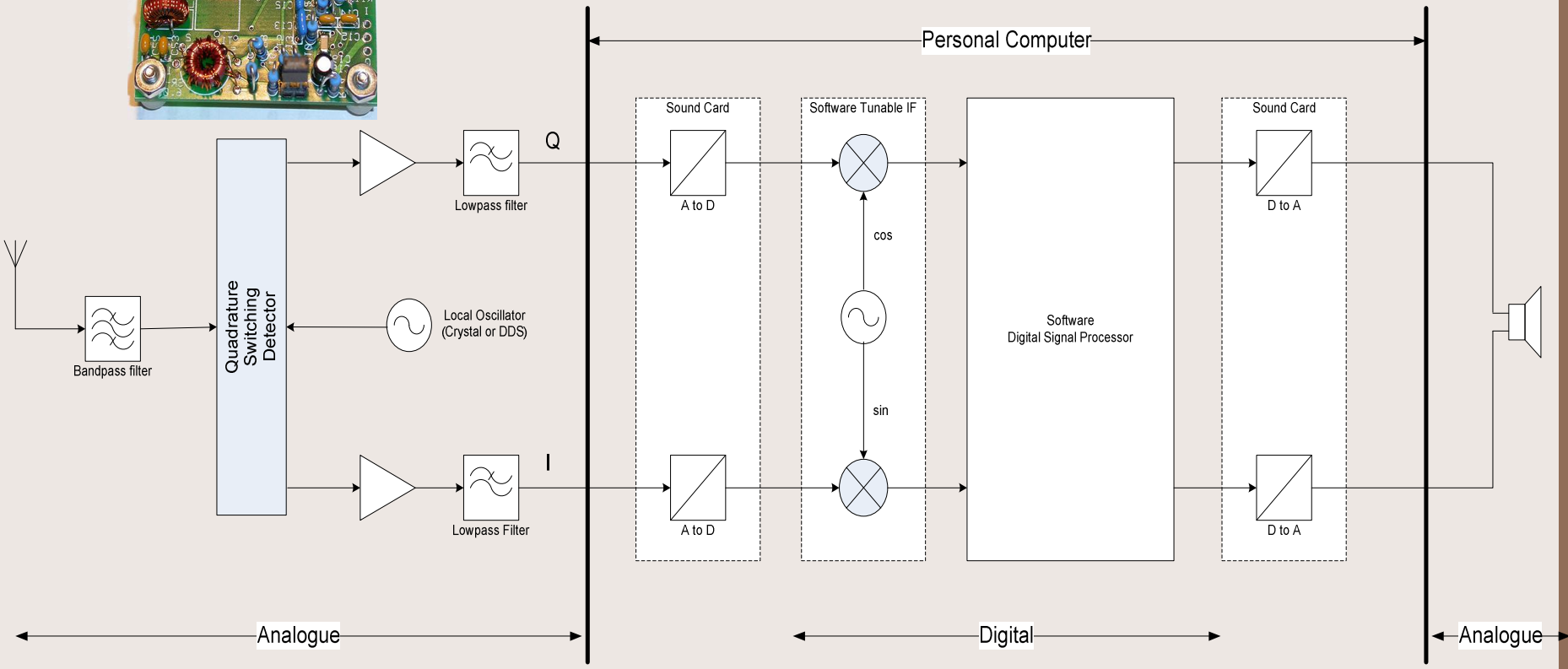
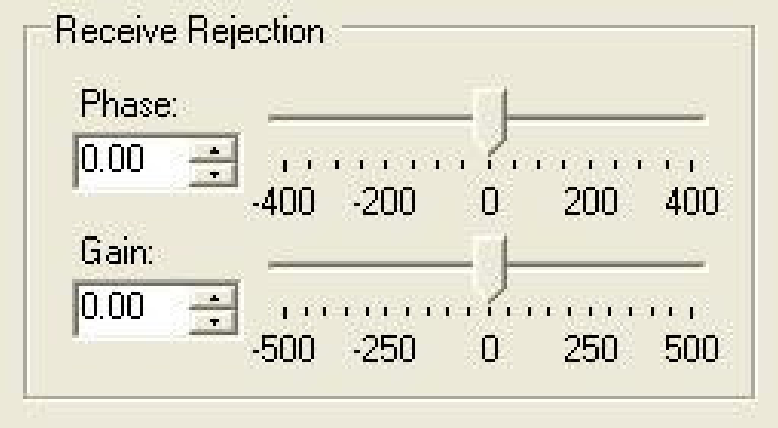


Figure 9 SoftRock Phasing Receiver

Are we there yet?

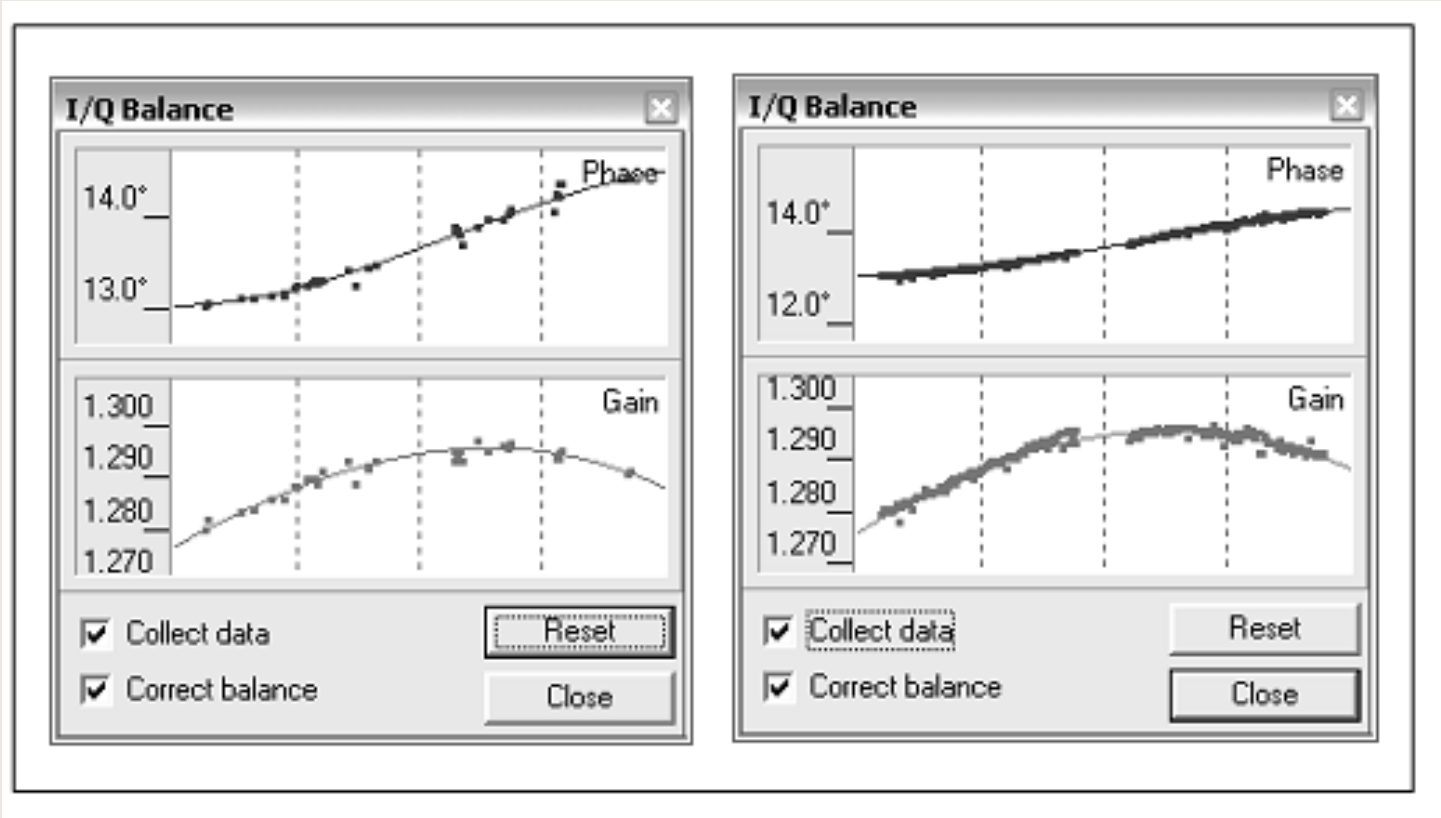
- Once inside the PC we can compensate for any I and Q phase or amplitude errors
- But what about all those analogue components before our soundcard ADC?
- They will degrade our image rejection
- But, we can compensate for ***consistent*** errors in the PC software

I & Q Error Correction



- Can provide >90dB of image rejection at a single frequency either manually or automatically
- But, image rejection will drop at band edges
- So, apply the correction at multiple frequencies

I & Q Error Correction



Switch on

After one day

'Rocky' software (Alex, VE3NEA) 'learns' how to correct I and Q using off-air signals

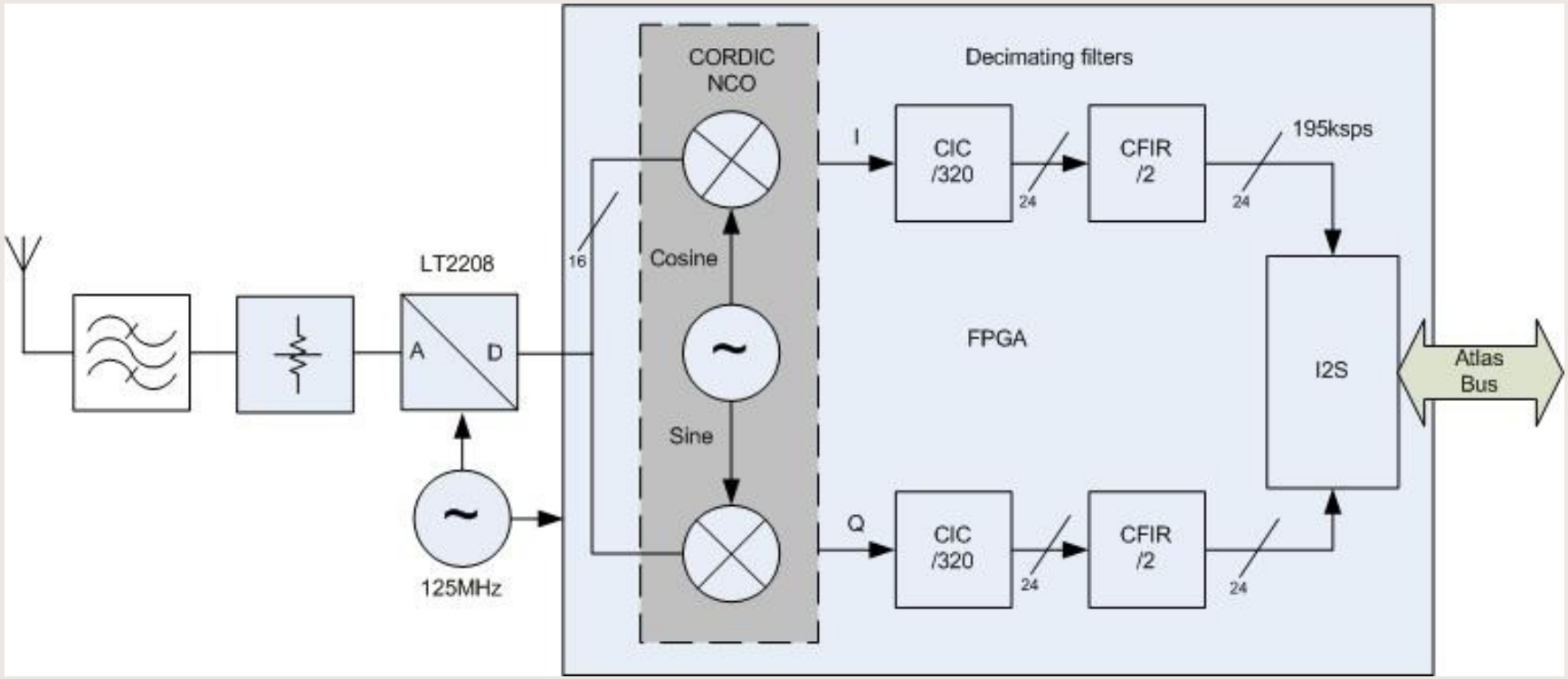
So, are we there now ?

- Not the full solution since:
  - We need enough, strong signals, for the calibration to work
  - The calibration will change with SWR, etc
  - Needs doing on each band
  - It's time consuming
- This doesn't mean it not a solvable problem

A fully digital solution

- If the analogue components prior to the ADC are the problem then why not get rid of them?
- With a high speed ADC we can do just that.
- The technique is called Digital Down Conversion (DDC).

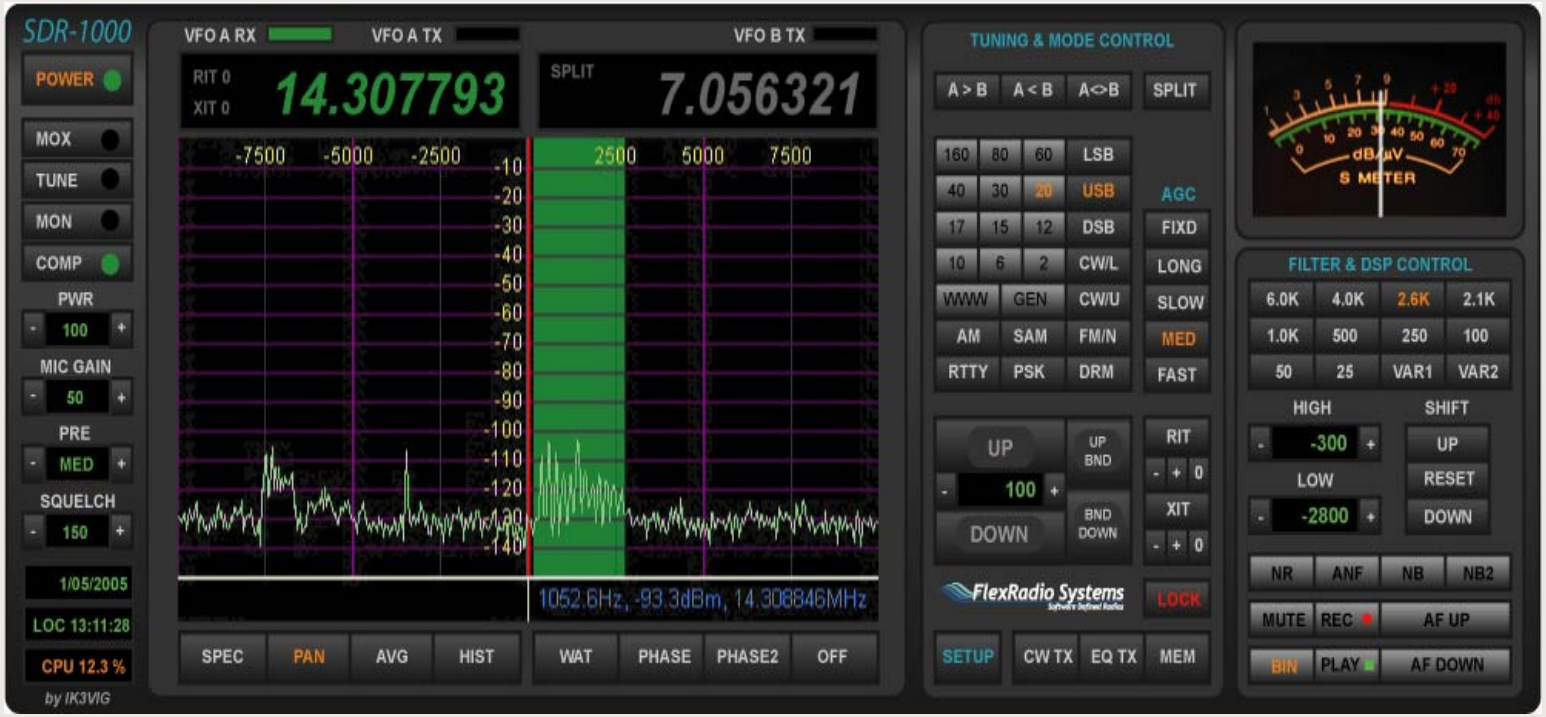
Digital Down Conversion



Summary

- Phasing techniques were popular in the early days of SSB
- The phase and amplitude accuracy requirements were too server in those days
- Using DSP we can achieve the required accuracies.
- Digital radios that use phasing techniques will be the way of the future

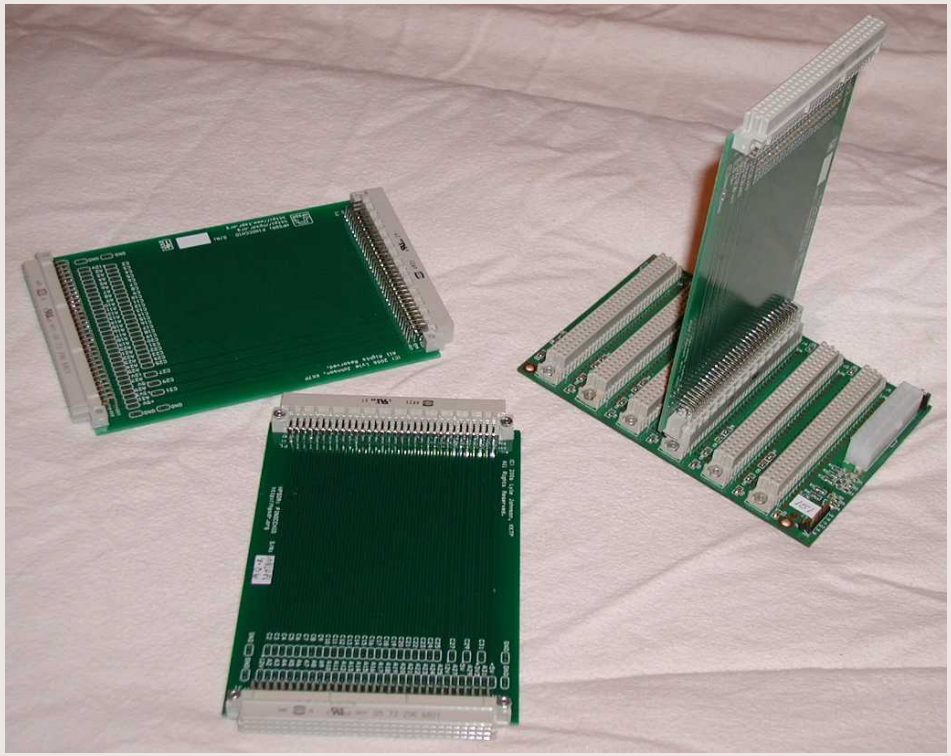
Questions?


SDR-1000
POWER
MOX
TUNE
MON
COMP
PWR
100
MIC GAIN
50
PRE
MED
SQUELCH
150
1/05/2005
LOC 13:11:28
CPU 12.3 %
by IK3VIG
VFO A RX
VFO A TX
VFO B TX
RIT 0
XIT 0
14.307793
SPLIT
7.056321
-7500 -5000 -2500 2500 5000 7500
-10 -20 -30 -40 -50 -60 -70 -80 -90 -100 -110 -120 -130 -140
1052.6Hz, -93.3dBm, 14.308846MHz
SPEC PAN AVG HIST WAT PHASE PHASE2 OFF
TUNING & MODE CONTROL
A > B A < B A<>B SPLIT
160 80 60 LSB
40 30 20 USB
17 15 12 DSB
10 6 2 CW/L
WWW GEN CW/U
AM SAM FM/N
RTTY PSK DRM
AGC
FIXD
LONG
SLOW
MED
FAST
UP
100
DOWN
UP BND
BND DOWN
RIT
XIT
FlexRadio Systems
LOCK
SETUP CW TX EQ TX MEM
S METER
FILTER & DSP CONTROL
6.0K 4.0K 2.6K 2.1K
1.0K 500 250 100
50 25 VAR1 VAR2
HIGH
-300
LOW
-2800
SHIFT
UP
RESET
DOWN
NR ANF NB NB2
MUTE REC AF UP
BIN PLAY AF DOWN

HPSDR

High Performance Software Defined Radio

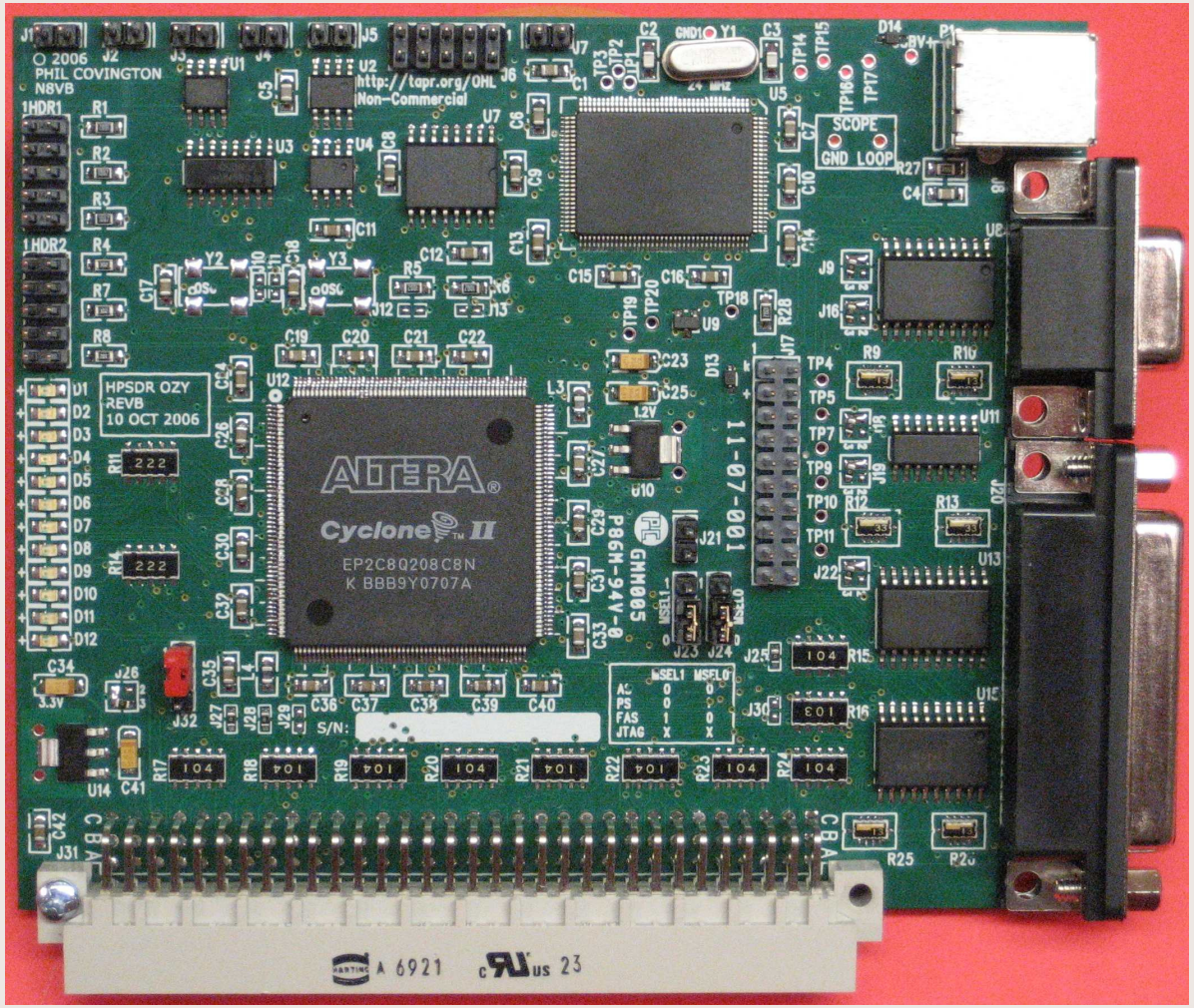
- Open Hardware and Software
- International development team
- Bulk purchase and non-profit
- Peer review of all items
- Developer support
- Currently Available
  - Atlas Bus
  - Pinocchio extender
  - Janus - Audio ADC/DAC
  - Ozy – USB interface
  - ~~Penelope – DUC exciter~~
- Future
  - Mercury – DDC receiver
  - Alex – HPF/LPF
  - Gibraltar – 10MHz high performance reference
  - Cyclops – 0 to 1GHz Spectrum Analyzer & Tracking Generator



ATLAS

HPSDR

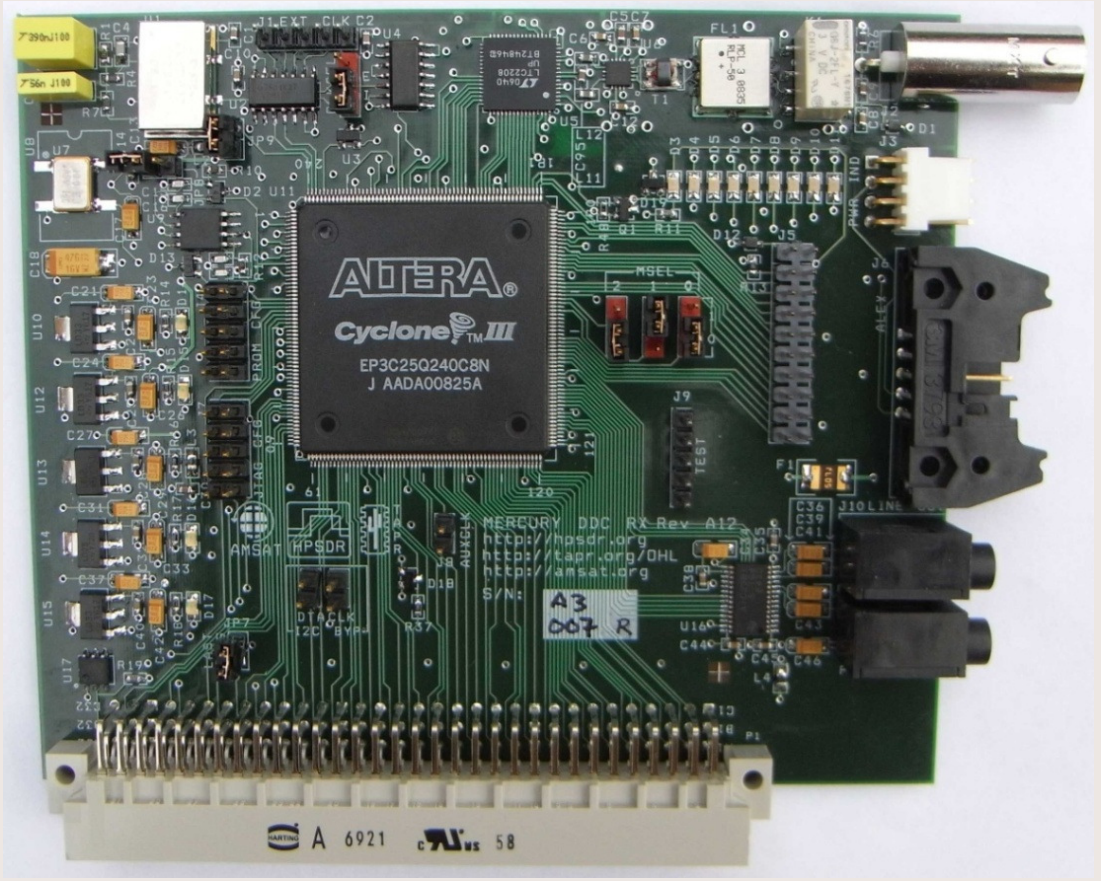
- USB 2 PC Interface
- Altera Cyclone II FPGA
- Parallel Port
- 2 x RS232
- Atlas Bus Interface
- Numerous I/O ports



OZY

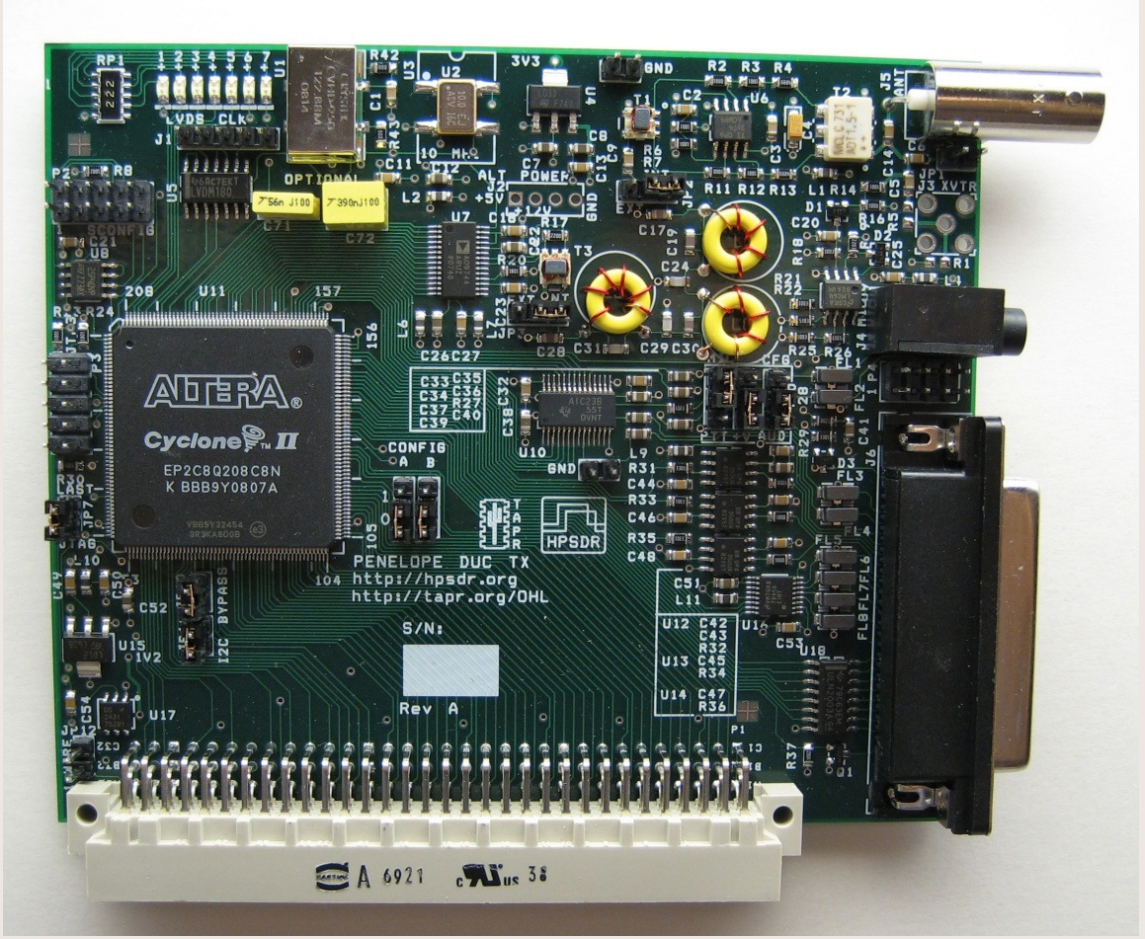
HPSDR

- Atlas Bus Interface
- LT2208 16bit 135Msps ADC
- 0-55MHz (alias to 700MHz)
- 10MHz TCXO/external ref
- -138dBm (500Hz)MDS
- Altera Cyclone III FPGA
- DDC in FPGA
- On board DAC for AF output



HPSDR

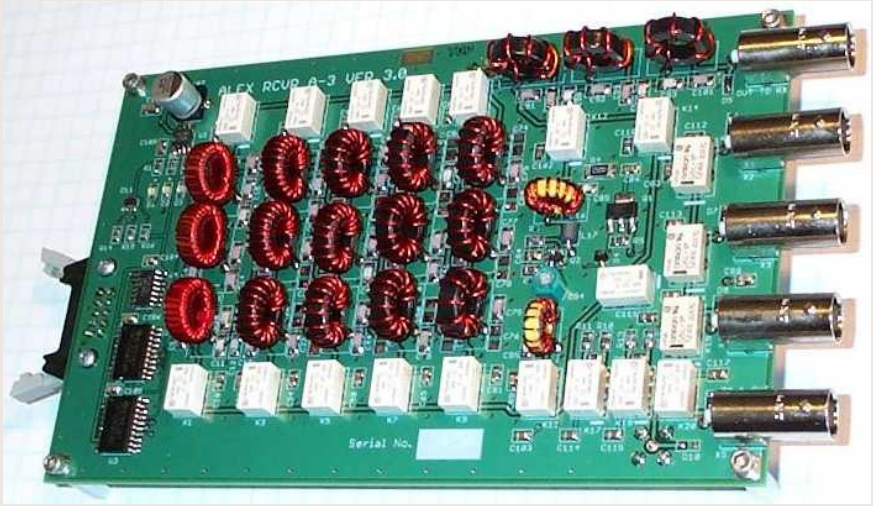
- Atlas Bus Interface
- 14bit 127Msps DAC
- 0-55MHz (alias to 450MHz)
- 10MHz TCXO/external ref
- 0.5W PEP Output
- Altera Cyclone II FPGA
- DUC in FPGA
- On board ADC for AF input



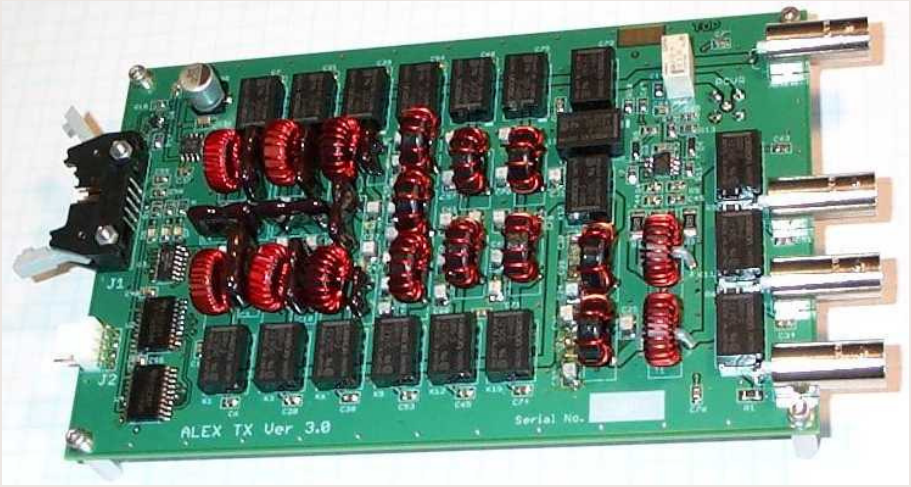
PENELOPE

HPSDR

- SPI Interface
- 160-6m Band Switched LPFs
- SWR bridge with log amps
- 6m Low Noise Pre-amp
- IP3 > +50dBm
- 3ms Tx/Rx switching

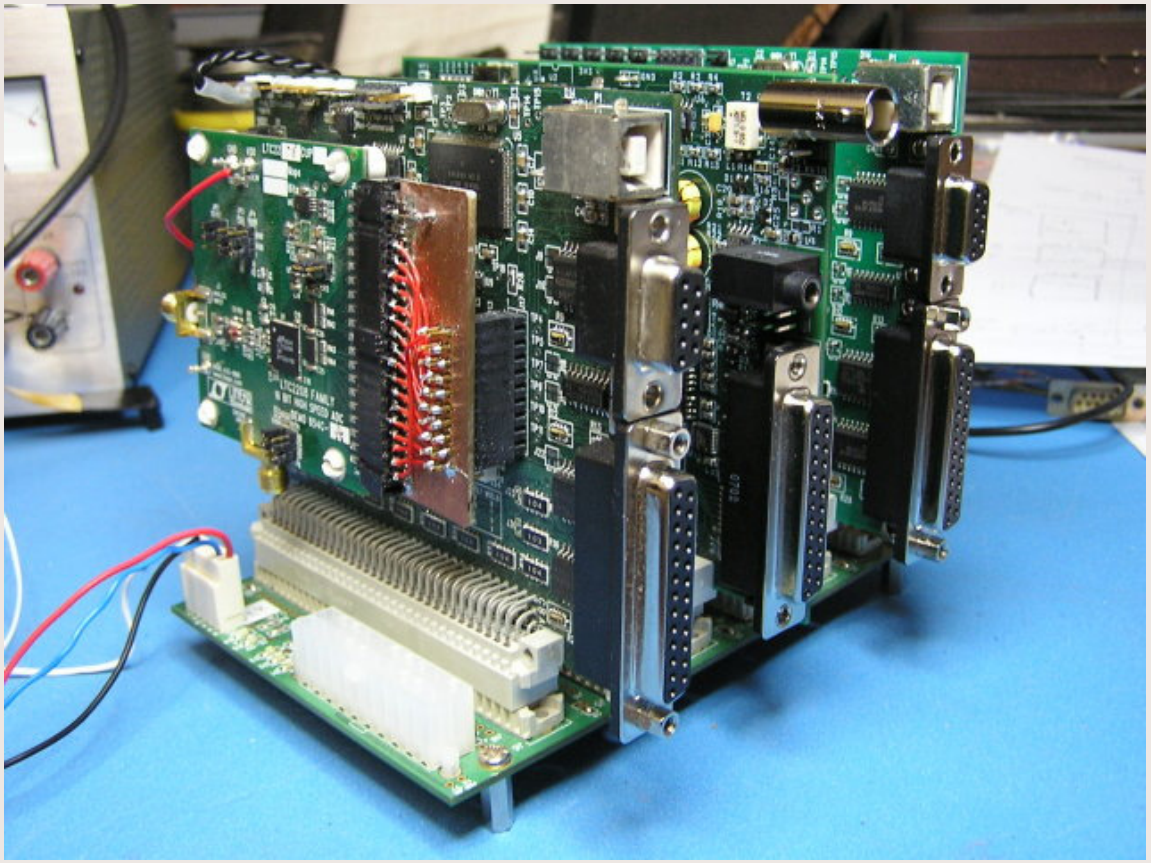


ALEX - HPF



ALEX - LPF

HPSDR



More Details: http://hpsdr.org